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CONTRACTOR REPORT

THE DEVELOPMENT OF A POWER SPECTRAL DENSITY PROCESSOR FOR C AND L BAND AIRBORNE RADAR SCATTEROMETER SENSOR SYSTEMS

(NASA-CR-171668) THE DEVELOPEMNT OF A POWER SPECTRAL DENSITY PROCESSOR FOR C AND L BAND AIRBORNE RADAR SCATTEROMETER SENSOR SYSTEMS (Lockheed Engineering and Management) 115 p HC A06/MF A01 CSCL 14B G3/35

N83-30993
Unclas
28398

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CONTRACT NAS 9-15800

FEBRUARY 1983

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HOUSTON, TEXAS

February 1983

Job Order 34-439
LEMSCO-19158

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FIGURES

FIGURES

ACRONYM LIST

ADC	Analog to Digital Converter
A/D	Analog to Digital Converter
ASCII	American Standard Code for Information Interchange
Bi-ϕ-L	Bi-Phase-Level
BPF	Band Pass Filter
CCD	Charge Coupled Device
CCT	Computer Compatible Tape
CPU	Central Processor Unit
CRT	Cathode Ray Tube
CZT	Chirp Z-Transform
DAC	Digital to Analog Converter
DFT	Discrete Fourier Transform
DIP	Dual Inline Package
EPROM	Erasable Programmable Read Only Memory
FCF	Functional Check Flight
FFT	Fast Fourier Transform
H	Hex
HH	Horizontal-Horizontal
H-P	Hewlett-Packard
I/O	Input/Output
I/V	Current to Voltage
LED	Light Emitting Diode
LSB	Least Significant Bit

ACRONYM LIST

MDAC	Multiplying Digital to Analog Converter
MSB	Most Significant Bit
NERDAS	NASA Earth Resources Data Annotation System
PROM	Programmable Read Only Memory
PSD	Power Spectral Density
RAM	Random Access Memory
R-C	Resistor-Capacitor
RMS	Root Mean Squared
SAL	Sensor Analysis Lab
SAR	Successive Approximation Register
SID	Serial Input Data
SOD	Serial Output Data
S/H	Sample/Hold
S/N	Signal to Noise
T and M	Timing and Multiply
USART	Universal Synchronous Asynchronous Receiver Transmitter
VV	Vertical-Vertical

ABSTRACT

A real-time signal processor was developed for the NASA/JSC L-and C-band airborne radar scatterometer sensor systems. The purpose of the effort was to reduce ground data processing costs. Conversion of two quadrature channels of data (like and cross polarized) was made to obtain Power Spectral Density (PSD) values. A chirp-z transform (CZT) approach was used to filter the doppler return signal and improved high frequency and angular resolution was realized. The processors have been tested with recorded signals and excellent results were obtained. CZT filtering can be readily applied to scatterometers operating at other wavelengths by altering the sample frequency. The design of the hardware and software and the results of the performance tests are described in detail.

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PSD PROCESSOR ANALOG SUBSYSTEM

SUMMARY

NASA, JSC in Houston,Tx has developed a real-time signal processor for the fan beam scatterometer system. The processor systems have been designed to process in real time two quadrature channel pairs of radar scatterometer signals from the NASA L-band (1.75 gHz) or C-band (1.60 gHz) systems. The processors have been implemented and tested in both L and C band flight systems using recorded radar and NERDAS signals as input data sources.

1.0 DESIGN OBJECTIVES AND OVERVIEW

The objectives of the scatterometer processing systems were to provide real time conversions of two channels of scatterometer data; like and cross polarized signals, into power spectral density (PSD) values. The hardware design features a chirp Z-transform (CZT) approach to filtering the Doppler spread radar return. The filtering operation reduces to that of performing a discrete Fourier transform (DFT) of the radar return when represented in complex value form. Each channel converts the quadrature signals into discrete PSD values

over the fore and aft Doppler spectra. Both are provided simultaneously with considerable reduction in circuit complexity, and sign sensing is not required.

There are many advantages to the CZT approach. It permits high frequency resolution of the Doppler return. As a consequence, the return may be measured with good angular resolution. This also permits the processor to adapt with changes in aircraft velocity to track the required viewing angles by simply using a different set of spectral outputs. It will also permit arbitrary choices in viewing angles if desired. The CZT approach can be readily applied to scatterometers operating at other wavelengths primarily by altering the sample frequency.

The power spectral density (PSD) of the total return is formed from the chirp Z-transform data. The formation of the PSD requires that the spectral data be detected (squared) and accumulated (averaged) over a period of time. To achieve the accuracy and the dynamic range required in scatterometry, the detection and accumulation is accomplished digitally. The detected and accumulated data is converted to estimates of the scattering coefficients sigma zero by significantly reduced ground station processing.

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2.0 SYSTEM ARCHITECTURE AND OPERATION

Each PSD processor has two channels to handle like and cross polarized return signals. Each channel converts the quadrature signals into discrete PSD values over the fore and aft Doppler spectra simultaneously. This operation is based on the CZT technique which may be reguarded as an analog technique of implementing the discrete Fourier transform (DFT). This operation is performed on a circuit board called an analog CZT card, one analog card for the like channel and one for the cross channel. The detection (squaring) and summation of like and cross channel spectral results is performed on another board called the timing and multiplier card. This card outputs total fore and aft PSD spectral values to the micro- processor controlled accumulator for both channels. A simplified block diagram is shown in Figure 2.0, and a more detailed block diagram is shown in drawing SIE 39115719.

The analog processor is contained in one card cage and consists of two analog cards and one timing and multiplier card. The digital processor inputs the multiplier outputs from each channel and accumulates the required number of PSD values to acquire a one-half second total. This results in 10 PSD cycles accumulated for each C-band processor output, and 5 PSD cycles

accumulated for each L-band processor output. The digital processor is in a separate card cage and contains two cards; the accumulator as just described, and a controller board that toggles the accumulator memory buffers, reads NERDAS, and outputs the data in a serial BI-Ø-L format at 100 kbps.

2.1 ANALOG CZT BOARD

This PSD system filters the fore and aft Doppler spectra of the radar return to form PSD values in 512 parallel spectral bins. Of these bins, 256 characterize the fore spectrum and 255 the aft spectrum. There is one bin which represents the nadir return, but this return is suppressed by the scatterometer equipment and the PSD processor. A sliding CZT algorithm is used to form repeated values of the power returned within each spectral bin. When the forward CZT is formed on the complex input signal x+jy, the aft spectrum appears in the first 255 accumulation bins and the fore spectrum appears in reverse order in the latter 256 bins. Ground return data is contained in these spectra along with calibration and polarization tones.

Analog Processor Subsystem

The analog board consists of four sections:

1) Input conditioning circuit,

2) Chirp multipliers and summers circuit,

3) Transversal filter and signal extraction circuit,

4) Analog to digital conversion and monitor circuit.

The block diagram is shown in Figures 2.1a and 2.1b. This analog circuit is built on a Mupac Corp. three section wire-wrap board p/n 3264890-03 with the passive components mounted on component carriers.

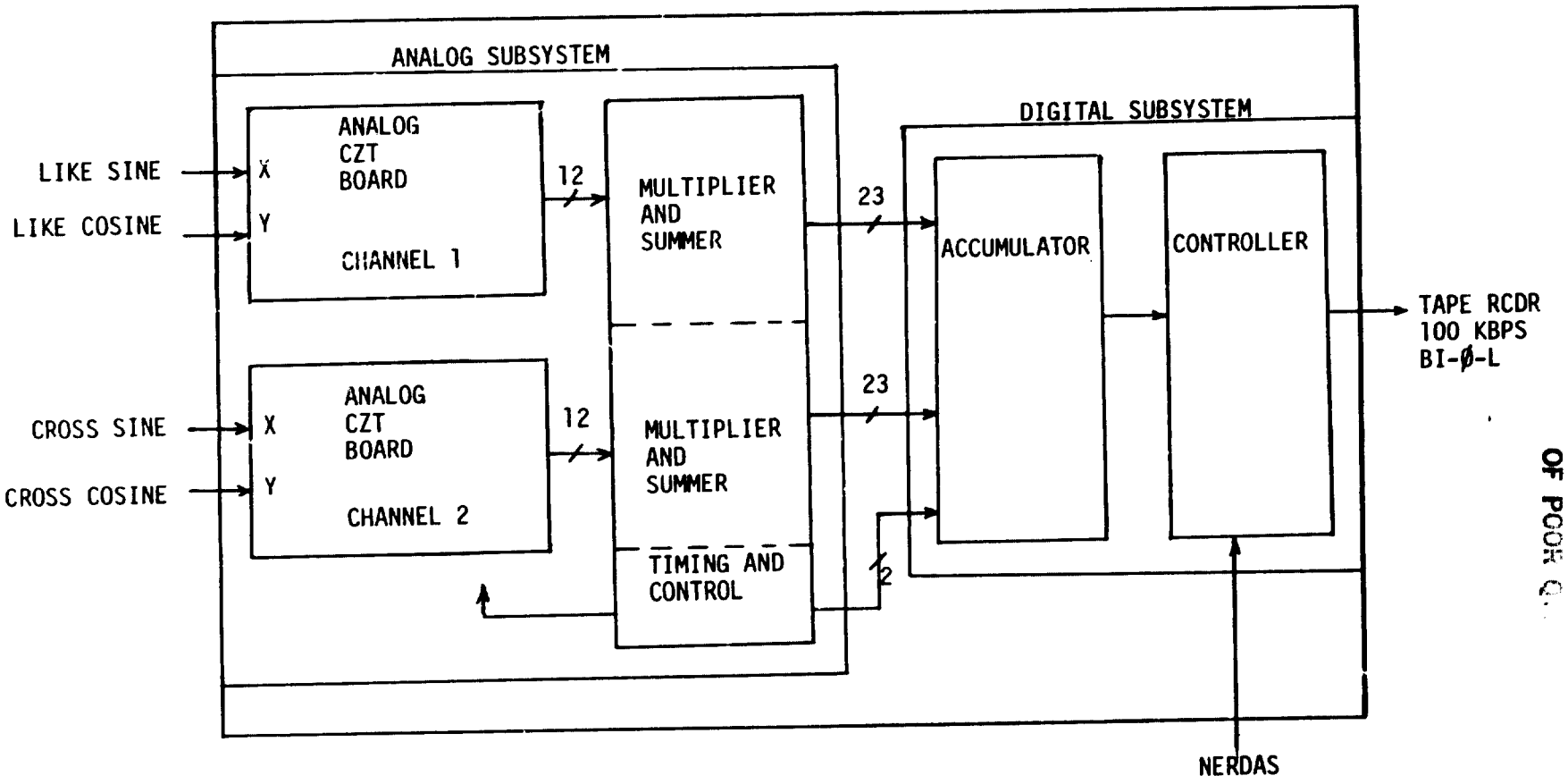

FIGURE 2.0 PSD SYSTEM BLOCK DIAGRAM

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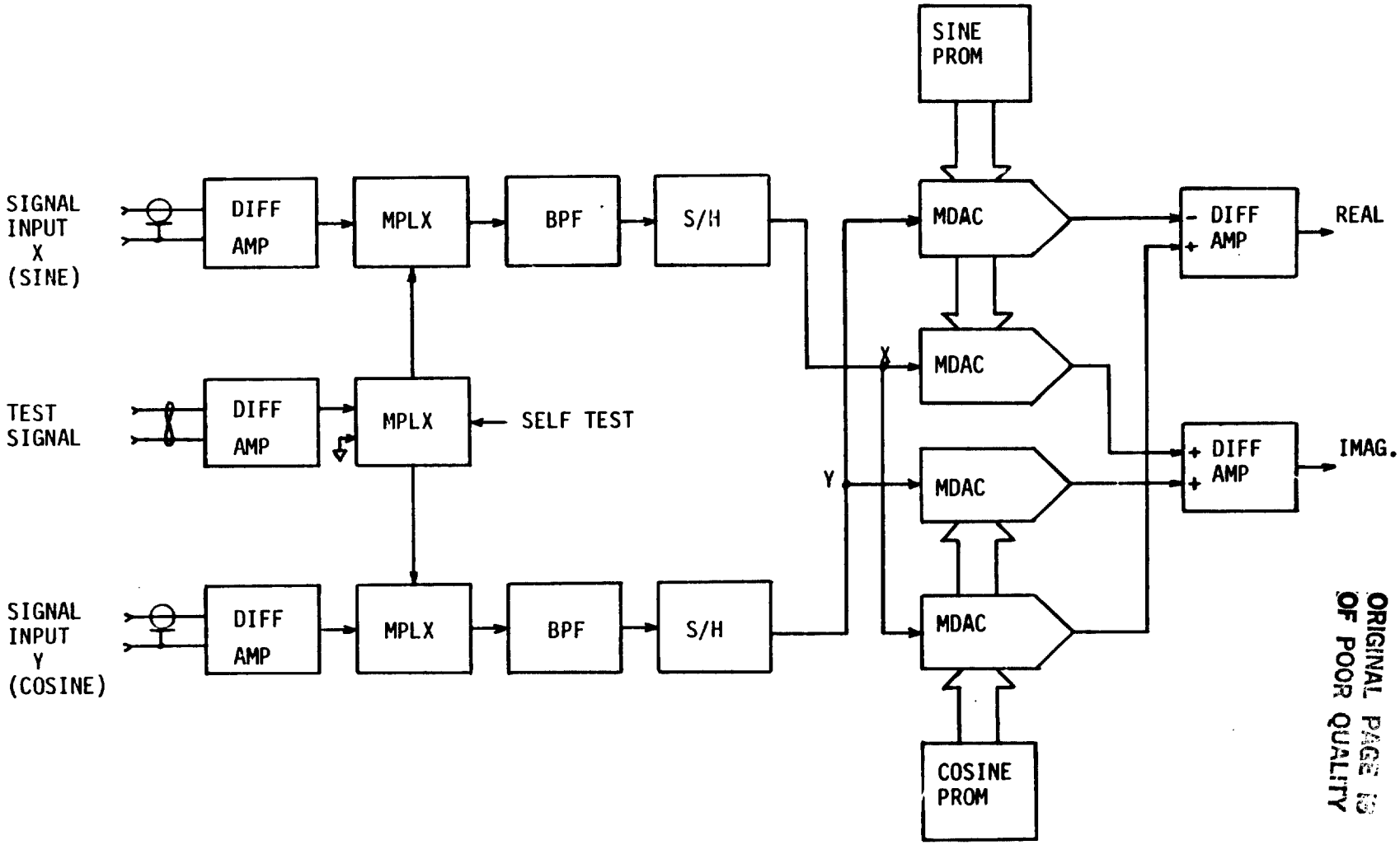

FIGURE 2.1(a) ANALOG CZT BOARD BLOCK DIAGRAM (PARTIAL)

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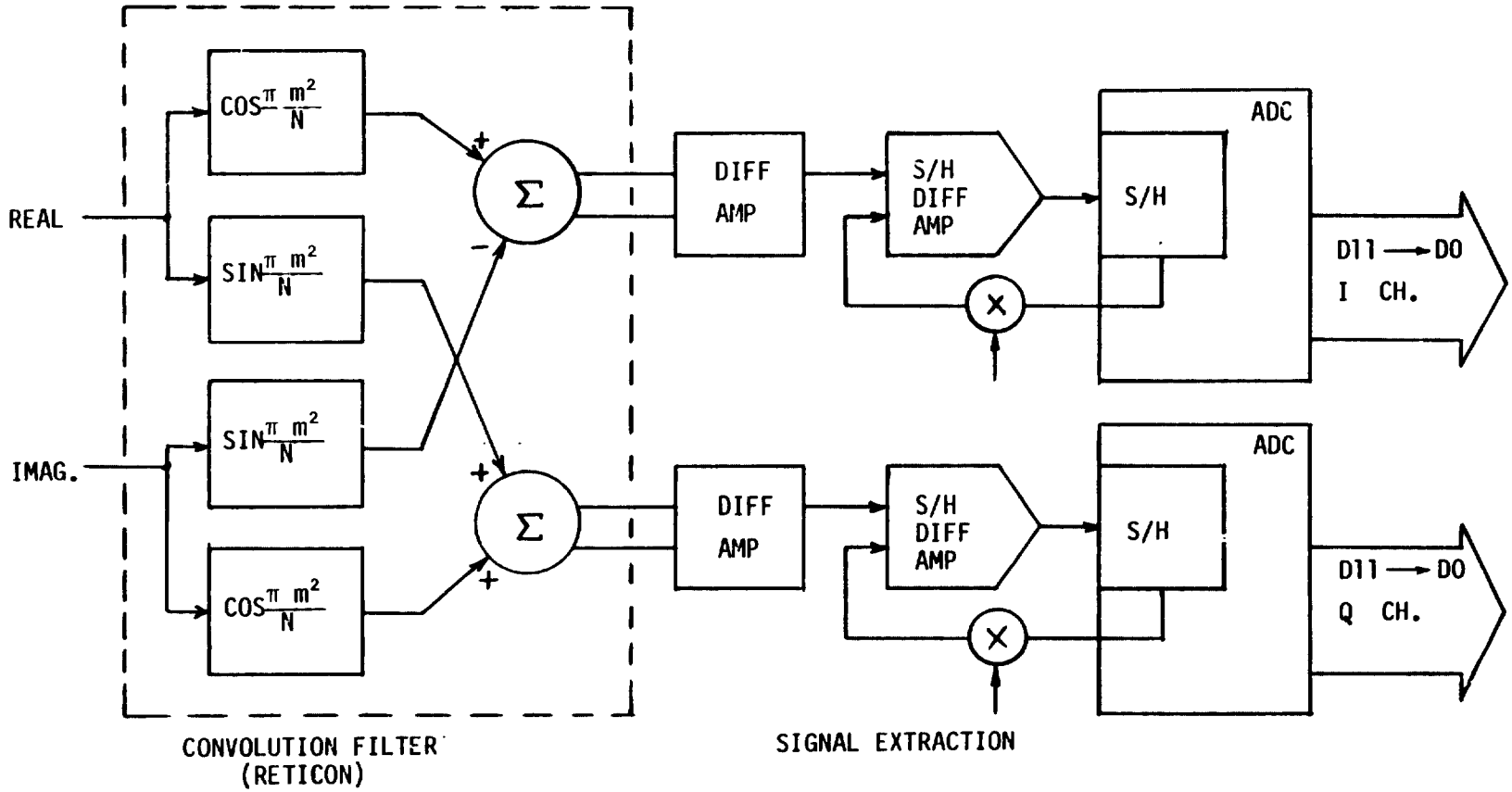

FIGURE 2.1(b) ANALOG CZT BOARD BLOCK DIAGRAM (Continued)

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2.1.1 INPUT CONDITIONING CIRCUIT

This description is on a card basis; recall that there are two identical channels (or cards) in the PSD processor for like and cross data. The analog cards input conditioning circuits consists of differential input amplifiers, analog switches, active bandpass filters, sample and hold circuits, and adjustable gain buffers as indicated in the block diagram on drawing SIE 39115719 and schematic drawing SIE 39115721, sheet 1.

Each analog card in the processor has two input channels, called X and Y in this discussion. Corresponding scatterometer signals may be called sine and cosine. The input signals are received in each channel by a differential amplifier to eliminate any common mode noise from the scatterometer system or through the cabling to the PSD processor. After this first amplifier, the signal paths are interruptable by an analog switch which can be selected to inject a test signal while the front panel SELF TEST switch is pressed. The signal paths then go through an ac coupled two pole high pass filter circuit to totally eliminate any dc or drift components induced by the scatterometers or from the tape recording system if playback data is processed. The data passband for the C-band scatterometer starts at 100 Hz, and at 30 Hz for the L-band.

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After the high pass filters, the signals then go through a four pole active low pass filter with characteristics similar to a Bessel filter. This type was choosen since balance and tracking of phase and gain are so critical throughout the passband of the system. The low pass filters are required to establish the processing bandwidth prior to sampling to avoid aliasing of high frequency noise components into the desired signal spectrum. The data passband for the C-band scatterometer goes up to 2.8 kHz, and up to 1.0 kHz for the L-band system.

A pair of adjustable gain amplifiers are then used to provide the required signal level to the follow on multiplying digital to analog converters (MDAC). It is important to operate the channels at the highest permissable amplitude to produce multiplications with good signal to noise (S/N) characteristics. It is also very important to match the gain throughout the passband in each parallel channel. Gain is now applied to increase the ratio of signal level to dc offset level in the hold mode of the sample and hold (S/H) circuit that follows. The S/H circuit converts the filtered input into a staircase approximation. This sampling is required to stabalize the amplitude for the subsequent pre-chirp multiplication and entry into the CCD transversal filter. The signal is sampled at a

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frequency about three times the highest calibration tone for each system. The calibration tones for the C-band scatterometer are at 2.93 kHz for HH polarization or at 3.38 kHz for VV polarization, and the PSD processor sample rate is 11.16 kHz. The calibration tone for the L-band scatterometer is at 1.9 kHz, and the PSD processor sample rate is 5.21 kHz. The polarization tone in the L-band scatterometer is higher in frequency than the calibration tone, but it is less than one-half the sample rate.

Following the S/H circuits are buffers for each of the two parallel channels, and these buffers have stable offset capability. These buffers are used in each input channel to prepare the X and Y signals for complex valued multiplication and summation. The offset levels must be suppressed to the millivolt level prior to multiplication at the pre-chirp operation.

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2.1.2 PRE-CHIRP MULTIPLIER AND SUMMERS CIRCUIT

The complex input signals must be multiplied by sine and cosine chirps and then algebraically summed. This is accomplished as shown in the schematic on sheet 2 of drawing SIE 39115721.

The MDAC's in conjunction with the current to voltage (I/V) converters and the programmable read only memories (PROM) are required to form the products required. An MDAC is composed of a precision resistive ladder network whose shunt currents are diverted into either of the two output ports where the proportional separation is dependent upon the digital input encoding. The output currents must be sunk into virtual grounds of the operational amplifier network as shown on sheet 2 in order for the I/V conversion to remain linear. The internal impedance of the MDAC's can vary 50% from a nominal value of 10 Kohm, and since they are in the feedback loop of the I/V converters, the output voltage is significantly affected by this variation. Therefore, it is extremely important to equalize the gain in each of the four MDAC stages in this circuit. Gain balance in the following summation circuits is also required, and this all is accomplished by selecting resistors in series with the inputs of the four MDAC's to equalize the entire circuits gains all the way through the summation and differencing circuits as shown in sheet 2

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of the schematic drawing. This process of gain balance is eased by the implementation of test switches on the analog board to disable the sine and cosine chirp PROM's outputs and to control these outputs to be individually selectable to values of all 1's or all 0's which correlate to sine and cosine values of +1 or -1. This allows for perfect gain balance by nulling outputs of the summing and differencing amplifiers. These switches are shown in sheet 3 of the schematic drawing.

After the X and Y signals are appropriately chirped, the summimg and differencing amplifiers are employed to form the real and imaginary parts required by the CZT algorithm. Prior to the summing and differencing operation, dc offsets are introduced into the real and imaginary channels as the CCD transversal filter requires that the chirped signals be offset on a positive voltage level.

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2.1.3 TRANSVERSAL FILTER AND SIGNAL EXTRACTION CIRCUIT

The real and imaginary parts of the chirped signals are injected into tne imaginary and real channels of the CCD transversal filter respectively, since the CCD filter is masked to perform the inverse DFT. This requires that the inputs be transposed to produce the forward transform as required by this design. Two transversal filters are required on each input to perform the complex valued convolution required by the CZT.

This circuitry is shown in the schematic on drawing SIE 39115721, sheets 2 and 4. The reversal in sign of one of the sine channels is purposely included in the bank of quad filters so that both of the output extraction circuit channels can be differentially connected. A differential connection is required because the convolution output must be extracted by pulsing the Ø1+ and Ø1- and the Ø3+ and Ø3- outputs through coupling capacitors Co. Once a differential output is pulsed, the capacitor acts as an integrating capacitor to receive the output charges from the transversal filters. Prior to receiving each new convoluted output, the previous output sample is discharged using MOSFET switches within the CCD chip. The switches are activated by the ØR1 and ØR3 signals. The combination of drive signals Ø1,Ø2,Ø3, and Ø4 are

required to move the input signals down the transversal filter. The timing diagram for these gating signals are shown in Figure 2.1.3.

An overview of the sampling and convolution operations can be established from the timing diagram. A basic input sample period is broken into 64 sub-periods and the different segments of sub-periods are allocated to the timing signals. A new BPF signal input sample is taken just prior to ØR3 going high. The ØR3 signal discharges the previous Ø3 output signals on Co. This input sample is pre-multiplied by the next chirp value clocked from the PROMs by CZTCLK. This pre-multiplied sample is loaded into the transversal filter with Ø2. Simultaneously Ø2 also latches the previous convolved output on the Ø3 channel into an analog output buffer. This output is extracted while Ø3 is high. At the end of the Ø3 signal, the previous Ø1 sample on the Ø1+ and Ø1- channels is discharged when ØR1 goes high. Then Ø4 latches the newly convolved output on the Ø1 channel in its output buffer. The Ø1 output is extracted while Ø1 is high. The cycle then repeats.

The two output channels contain the real and imaginary values of the DFT of the complex valued input signal except for a constant phase factor between the two channels. The output voltage is held by the integrating capacitors and buffered prior to being

operated on by a sampling differential amplifier. The integrating capacitors must be very well balanced to retain the common mode rejection required to extract the signal off the voltage pulses out of the CCD filter. The following differential amplifier samples and holds the differential value from the pulsed outputs of the CCD filter and amplifies it.

The Ø1 channel has an additional S/H to bring that channel into synchronization with the Ø3 channel. The S/H stages also function to remove the residual common mode signal. This signal would appear as a dc offset at the output of the channels if no dc compensation were employed. However, to remain calibrated at the output, a dc stabilization loop has been included to restore the noise floor level to zero volts. This is accomplished by integrating the signal level in 32 bins that are centered at the crossover frequency of the sampled system and using this level as negative feedback to keep the average noise floor at zero volts. The input complex signal should have no data or signal content at this highest frequency spectra.

A null adjustment is available in each channel to achieve this condition. The negative feedback is very essential in removing and stabalizing the dc component before digital conversion and multiplication, and allows the output channels to operate over the full dynamic

range of 60 dB. It is important to employ low-noise operational amplifiers with high slew rate and large input common-mode voltage range at the outputs of the CCD transversal filter to realize the inherent dynamic range of the filter. The large bandwidth amplifiers then require the differential S/H stages to be followed by low pass amplifiers to reduce the noise bandwidth without affecting the signal bandwidth.

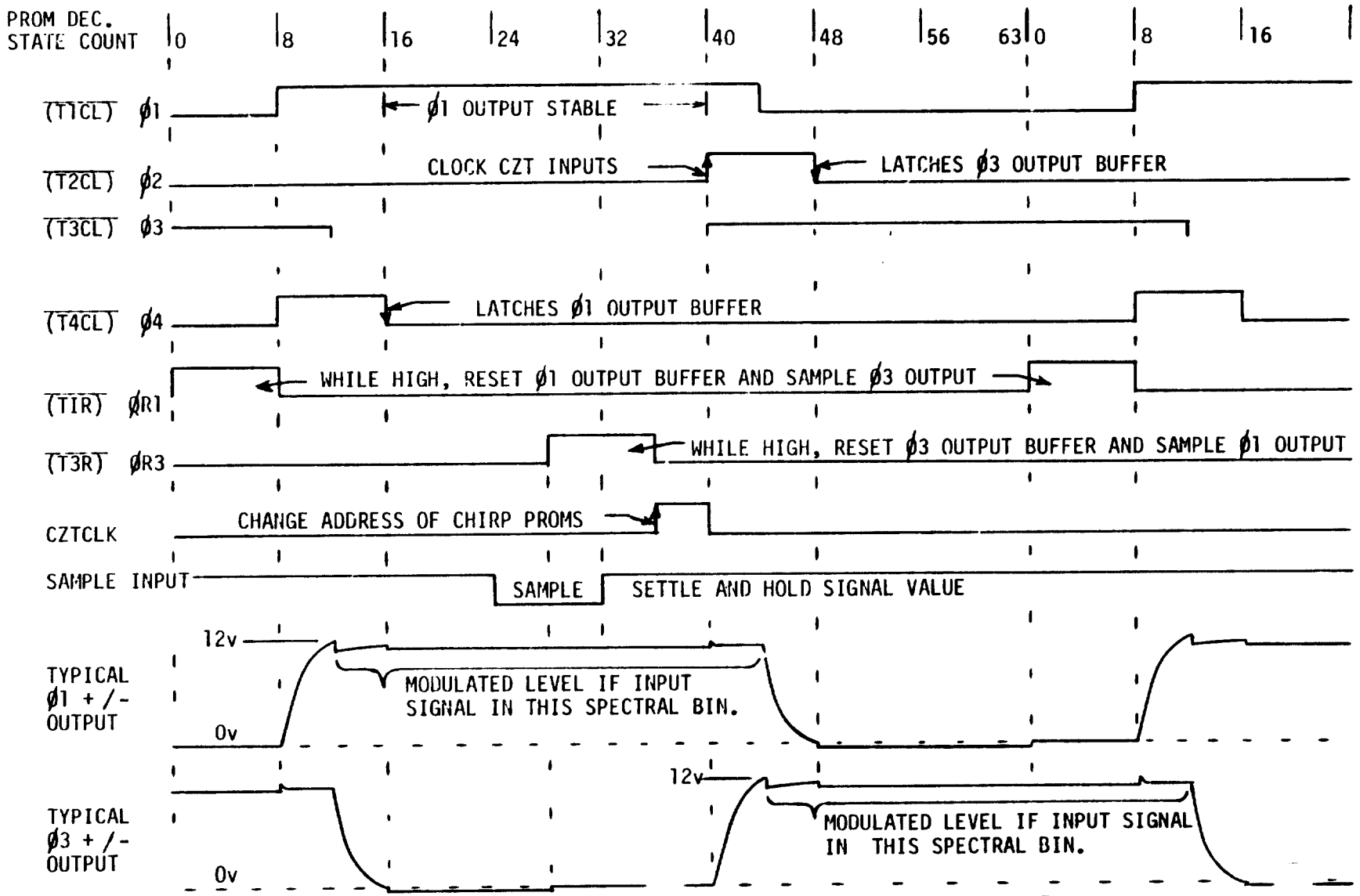

FIGURE. 2.1.3 TIMING DIAGRAM FOR CZT FILTER AND EXTRACTION CIRCUIT.

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2.1.4 ANALOG TO DIGITAL CONVERSION AND MONITOR CIRCUIT

The output of each I and Q channel is digitized by a 12 bit successive approximation register (SAR) analog to digital converter (ADC). This converter has an internal S/H so the preceding circuit does not have to drive the dynamic SAR input circuit, and this S/H is within the zero restorer feedback loop. Since the input signal is bipolar, this ADC allows conversion to 11 bits accuracy with the most significant bit (MSB) being a sign bit. The output of the converter is complementary offset binary but the analog boards output is converted to 2's complement by inverting the lower 11 bits, as shown in drawing SIE 39115721, sheets 4 and 5. This is preparatory to driving the multiplier circuit on the T&M board. A timing diagram is shown in Figure 2.1.4.

To aid in understanding and testing the analog board, a digital to analog converter (DAC) was added to "view" the total analog circuitry performance by reconstructing the digitized output back into an analog format. It can be selected to output the analog response of the real or the imaginary channel, and is very useful for nulling the dc outputs prior to multiplication and for noise analysis.

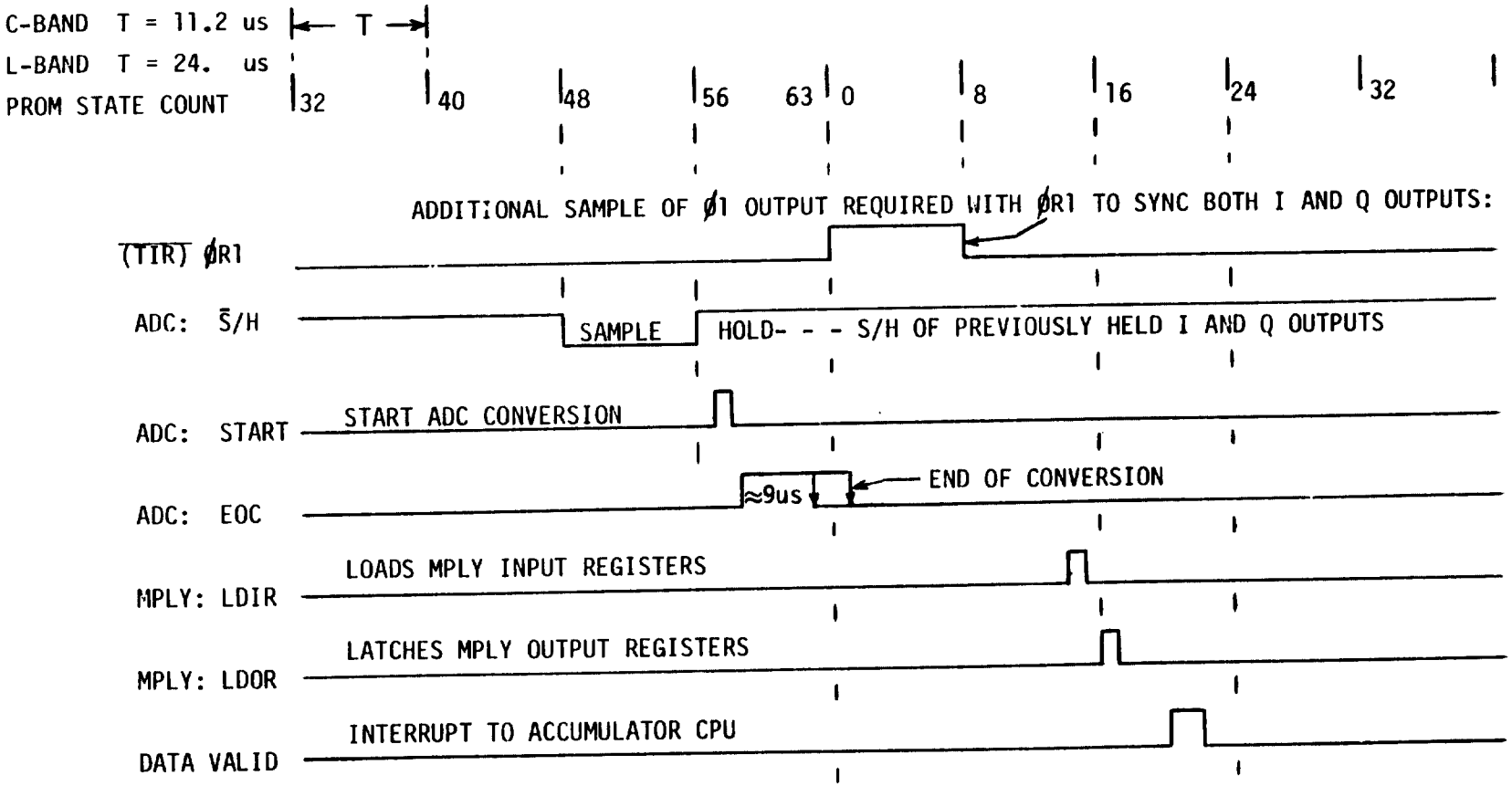

FIGURE 2.1.4 TIMING SIGNALS FOR SIGNAL PROCESSING

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2.2 TIMING AND MULTIPLIER BOARD

All system timing for the analog chirp Z-transform circuit and for the multiplier sections on this board are generated in the timing section on this board. Detailed description of the operation are presented in the following sections.

2.2.1 TIMING GENERATOR

The timing circuit provides all timing and control signals for the analog CZT board, the multiplier sections, and provides interrupts to the CPU in the digital processor section. A schematic diagram is shown in drawing SIE 39115723, sheet 1.

The timing signals originate from a 5 MHz crystal oscillator, and this signal is divided down by a fixed divider to form a master clock frequency called MCLK. The division is by 7 for the C-band and by 15 for the L-band unit. MCLK then drives a continuously running 64 state controller which also provides the system sampling rate, which is 11.16 KHz for the C-band and 5.208 KHz for the L-band unit. The 64 state controller is clocked by a six bit counter whose outputs provide addressing for the 64 state controller PROM's. There are 16 different state control signals generated by the controller PROM's. These state control signals are

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buffered by the MCLK signal to eliminate transition noise from the PROM outputs and to synchronize all output transitions. Of the 16 state control signals, 6 are clock signals which operate the CCD transversal filter, one is used to sample the input analog signal, 2 are used for A/D conversion, 2 are used for multiplication, 2 are used as interrupts for the CPU accumulator, another is used to clock the chirp PROM's, and the remaining 2 are alternate but unused signals. The coding for the 64 state PROM's are listed in Figure 2.2.1, and the timing signals have been shown in Figures 2.1.3 and 2.1.4.

The six analog control signals are identified in Figure 2.2.1 as T1CL to T4CL, T1R, and T3R. These signals are supplied to the analog CZT board, which in turn generate the signals Ø1 to Ø4, ØR1, and ØR3 as described in section 2.1.3. The signal CZTCLK increments a 9 bit chirp PROM address counter, whose resulting address signals RA0 to RA8 select the appropriate chirp waveform value to be multiplied with the sampled input signals as the first step in performing the discrete Fourier transform (DFT).

The signal FRAME is gated with PSD spectral bin count of zero to provide an interrupt to the CPU accumulator for FRAME START, and the signal DATA VALID is also sent as an interrupt to the CPU accumulator for

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		PROM T2									PROM T1								
DEC STATE	HEX STATE	HEX CODE →	SAMPLE INPUT	ALT CZTCLK	FRAME START	DATA VALID	START	S/H	LDIR	LDOR	CZTCLK	T1CL	T2CL	T3CL	T4CL	T1R	T3R	$\overline{DTEN}$	← HEX CODE
0	0	84	1	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1	6B
1	1	84	1	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1	6B
2	2	84	1	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1	6B
3	3	84	1	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1	6B
4	4	84	1	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1	6B
5	5	84	1	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1	6B
6	6	84	1	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1	6B
7	7	84	1	0	0	0	0	1	0	0	0	1	1	0	1	0	1	1	6B
8	8	84	1	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	27
9	9	84	1	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	27
10	A	84	1	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	27
11	B	84	1	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	27
12	C	84	1	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	37
13	D	84	1	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	37
14	E	86	1	0	0	0	0	1	1	0	0	0	1	1	0	1	1	1	37
15	F	84	1	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	37
16	10	85	1	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	3F
17	11	84	1	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	3F
18	12	84	1	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	3F
19	13	84	1	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	3F
20	14	94	1	0	0	1	0	1	0	0	0	0	1	1	1	1	1	1	3F
21	15	94	1	0	0	1	0	1	0	0	0	0	1	1	1	1	1	1	3F
22	16	84	1	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	3E
23	17	84	1	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	3E

FIGURE 2.2.1(a) TIMING PROM CODING

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		PROM T2									PROM T1								
DEC STATE	HEX STATE	HEX CODE →	SAMPLE INPUT	ALT CZTCLK	FRAME START	DATA VALID	START	S/H	LDIR	LDOR	CZTCLK	T1CL	T2CL	T3CL	T4CL	T1R	T3R	$\overline{DTEN}$	HEX CODE ←
24	18	04	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	3E
25	19	04	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	3E
26	1A	04	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	3E
27	1B	04	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	3E
28	1C	04	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	3C
29	1D	04	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	3C
30	1E	04	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	3C
31	1F	04	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	3C
32	20	C4	1	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0	3C
33	21	C4	1	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0	3C
34	22	C4	1	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0	3C
35	23	C4	1	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0	3C
36	24	84	1	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	BF
37	25	84	1	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	BF
38	26	84	1	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	BF
39	27	84	1	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	BF
40	28	84	1	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	0F
41	29	84	1	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	0F
42	2A	84	1	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	0F
43	2B	84	1	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	0F
44	2C	84	1	0	0	0	0	1	0	0	0	1	0	0	1	1	1	1	4F
45	2D	84	1	0	0	0	0	1	0	0	0	1	0	0	1	1	1	1	4F
46	2E	84	1	0	0	0	0	1	0	0	0	1	0	0	1	1	1	1	4F
47	2F	84	1	0	0	0	0	1	0	0	0	1	0	0	1	1	1	1	4F

FIGURE 2.2.1(b) TIMING PROM CODING

Lockheed

		PROM T2									PROM T1								
DEC STATE	HEX STATE	HEX CODE →	SAMPLE INPUT	ALT CZTCLK	FRAME START	DATA VALID	START	S/H	LDIR	LDOR	CZTCLK	T1CL	T2CL	T3CL	T4CL	T1R	T3R	$\overline{DIEN}$	← HEX CODE
48	30	84	1	0	0	0	0	1	0	0	0	1	1	0	1	1	1	1	6F
49	31	84	1	0	0	0	0	1	0	0	0	1	1	0	1	1	1	1	6F
50	32	80	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	6F
51	33	80	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	6F
52	34	80	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	6F
53	35	80	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	6F
54	36	80	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	6F
55	37	80	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	6F
56	38	80	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	6F
57	39	80	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1	1	6F
58	3A	84	1	0	0	0	0	1	0	0	0	1	1	0	1	1	1	1	6F
59	3B	AC	1	0	1	0	1	1	0	0	0	1	1	0	1	1	1	1	6F
60	3C	A4	1	0	1	0	0	1	0	0	0	1	1	0	1	1	1	1	6F
61	3D	84	1	0	0	0	0	1	0	0	0	1	1	0	1	1	1	1	6F
62	3E	84	1	0	0	0	0	1	0	0	0	1	1	0	1	1	1	1	6F
63	3F	84	1	0	0	0	0	1	0	0	0	1	1	0	1	1	1	1	6F

FIGURE 2.2.1(c) TIMING PROM CODING

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each spectral bin value.

Also included on this timing board is a function generator chip to send a sine wave into the front end of the PSD processor while the front panel SELF TEST button is pressed. The oscillator frequencies are approximately 810 Hz for the C-band and 380 Hz for the L-band.

2.2.2 MULTIPLICATION, SUMMATION, AND PSD MONITOR DAC

The Timing and Multiplication (T&M) card contains two duplicate sections of I and Q signal multipliers, summation circuits, and parallel outputs to the digital processor chassis for like channel data and for cross channel data. The digitized I and Q outputs from each analog card represent the real and imaginary parts of the DFT of the complex valued input signals. To convert these to a PSD, the real and imaginary parts must be squared, and summed for each spectral bin, or line. Detection (squaring) and summation are accomplished digitally as shown in the block diagram of Figure 2.0 and in the schematic diagrams in drawing SIE 39115723, sheet 2.

The 12 bit parallel data from an I channels ADC output and from a Q channels ADC output from one of the analog CZT boards are input in 2's complement format

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into the LSI parallel multipliers. The I channels parallel data are input simultaneously into one multipliers X and Y inputs, resulting in a 22 bit product. The same task is employed for the Q channels parallel data, which also results in a 22 bit product. These two products, being the real and the imaginary PSD values are then summed by six adder chips that produce a 23 bit result. This summed result, along with the other channels result, is then output to the CPU controlled accumulator and controller, also called the digital processor, and a certain number of spectral frames are accumulated to form a one-half second average of PSD.

The time period for a spectral frame to occur out of the C-band analog processor is the number of spectral lines (512) per frame divided by the input sampling frequency (11.16 KHz) which results in a frame time of 45.88 ms. The frame time for the L-band analog processor is 512 divided by 5.208 KHz which results in 98.3 ms. Therefore, to acquire one-half second averaged data, the following digital processors accumulate 10 spectral frames of the C-band analog data, and 5 frames of the L-band analog data.

Also contained with each of the two seperate channels multiplier and summation circuits is a digital to analog converter (DAC) to allow reconstruction of the digitized values of the PSD spectrum. This allows a

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display of the input signal power with respect to frequency, similar to a spectrum analyzer. Such an analog output signal is provided for each of the data channels; the like channel and the cross channel. The data is reconstructed from the 23 bit data word using the most significant 16 bits, excepting the carry bit. Since this output is the squared and summed value of the real and imaginary data, only the highest levels of signals are observable, whereas the lower level signals and noise floor are not, due to the output being a linear representation of the squared results and not logarithmic. These outputs are called PSD MONITOR OUTPUT for each channel. Also provided is a sync output signal for oscilloscope triggering. These outputs are available at the back of the processors chassis on BNC connectors.

The DAC is preceded by a digital multiplexer circuit to allow the DAC to convert one of three digital signals. The selection is accomplished by an on the board dual inline package (DIP) switch. The three selectable signals are 1) the squared and summed product of I and Q, also considered the PSD value and the most desirable signal to monitor, 2) the squared product of I, or 3) the squared product of Q. The last two of the selectable signals are useful for analyzing each part of the channels response, and for testing and calibration.

On the engineering board only, is an additional DAC circuit that is very useful for setting the analog zero level for noise floor. Since this parameter is so critical for minimizing the noise floor level, this test DAC should be used for adjustment of the offset null potentiometers on the analog cards. The input to this DAC is on connector P4, pins X29 for MSB through X36 for LSB, with the DAC output voltage on pin X27. Also on this board only, the lower 8 bits of each of the four LSI multiplier outputs is wired to connector P5. By using an 8 pin in line connector, the test DAC input can be jumpered to each of the four multipliers lower order 8 bits in order to set the pre-digitized level to minimize the squared value for the no input signal noise floor. This test DAC is shown on sheet 3 of the schematic of the T&M board, drawing SIE 39115723.

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3.0 TESTS AND RESULTS OF THE PSD PROCESSORS

Each PSD processor was tested as a system with the output data collected on an instrumentation tape. Therefore the analog subsystem was outputing parallel data at the frame rate, and the digital processor subsystem was accumulating the frame data and outputing the BI-Ø-L data including NERDAS at 100 Kbps to the tape recorder.

3.1 TEST SYSTEM

The test system was set up as shown in Figure 3.1 with an input source to the PSD processor being an Hewlett-Packard (H-P) variable phase function generator model 203A. To monitor the sources output, an H-P gain phase meter model 3575A was used. The data was recorded on an Ampex AR1700 14 track instrumentation tape recorder, with a tape speed of 15 ips.

The taped test data was decommed at the Lockheed supported NASA-JSC Sensor Analysis Lab (SAL) in building J15 using a PDP-11/70 to process and tab out the actual PSD count values in hex. This information was transfered to a CCT which then could be input to a VAX for logarithmic conversion to decibel (dB) and for plotting of the spectral data.

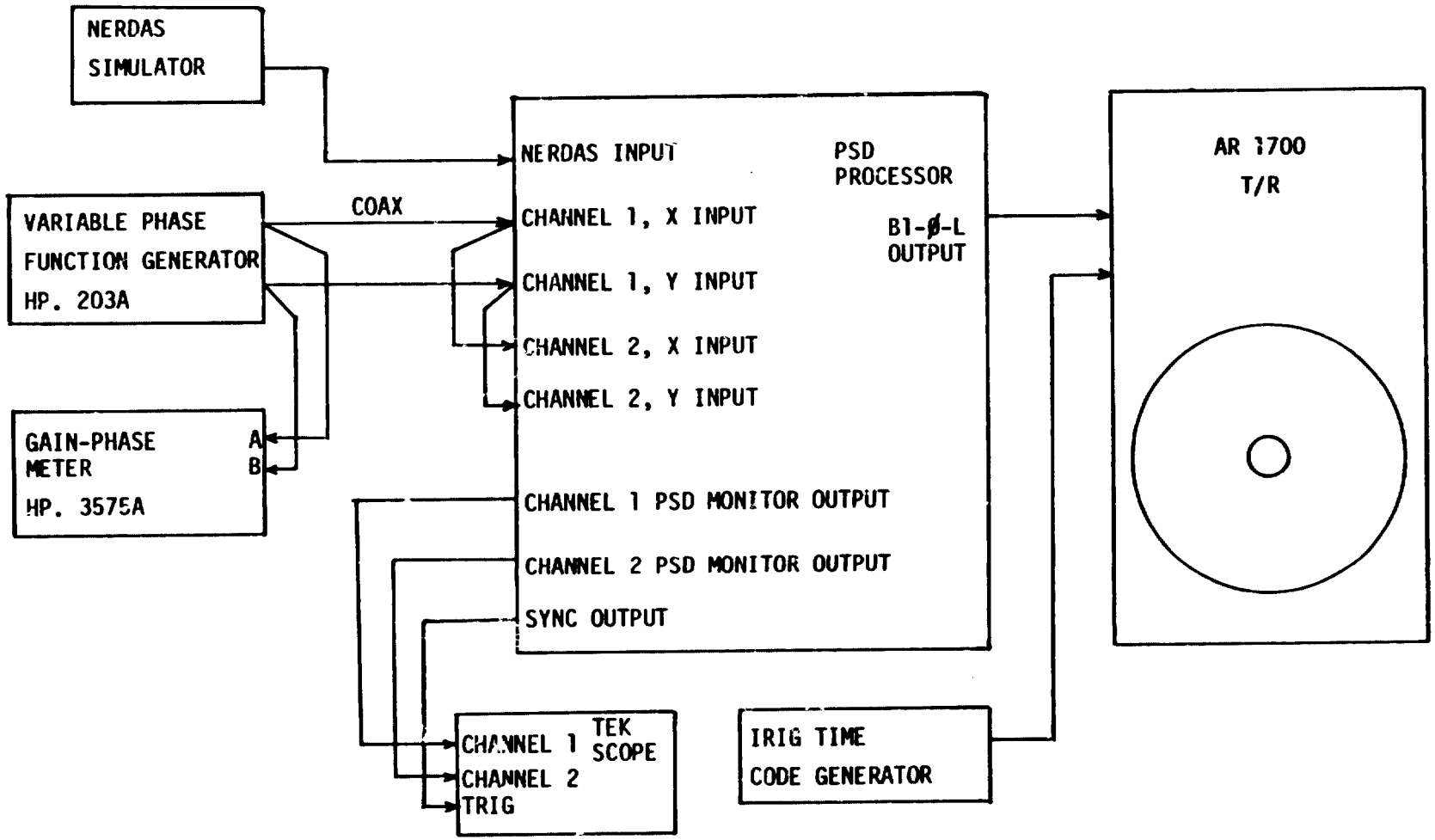

FIGURE 3.1 TEST SYSTEM

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The types of tests that were run on the PSD processor were:

1) dynamic range and linearity
2) signal frequency response
3) gain balance
4) fore and aft signal separation (isolation)
5) phase balance

Discussions of each test follows.

3.2 DISCUSSION OF C-BAND TESTS AND RESULTS

The first test run was for dynamic range and linearity of the PSD processor. A tone of approximately 1 KHz was injected into one channels X and Y inputs simultanously over a range of greater than 60 dB. The input frequency was adjusted slightly to assure that the input signal was centered in one spectral bin of the processor by viewing the MONITOR OUTPUT on an oscilloscope. The data that was taped performed its normal accumulation of 10 frames of analog PSD data for the intended one-half second averages. Typical spectral plots are shown in Figures 3.2.1 for a large input signal and in 3.2.2 for a lower signal at 40 dB below the first figure. A plot of dynamic range and linearity results from the converted data is shown in Figure 3.2.3 where the peak spectral amplitudes in dB were correlated with the input signals also measured in dB. From this plot it is apparent that the system exhibits a linear

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input power to output power relationship over a greater than 60 dB dynamic range. The same test was then performed for the second channel.

The next test determined the frequency response envelope of each X and Y signal path for both the like (channel 1) and cross (channel 2) data channels. The signal source was set at a mid-band frequency of 1 KHz and the input level set several dB below maximum. Data was tape recorded for about 28 different frequencies throughout the passband of the system. The tabulated data is plotted in Figures 3.2.4 and 3.2.5 for channels 1 and 2. The C-band scatterometer signal data bandwidth is from 100 Hz to 2800 Hz, the HH calibration tone is at 2930 Hz, and the VV cal tone is at 3380 Hz. The ripple across the input filter was not to exceed +/- 0.5 dB over the data bandwidth, and this requirement was satisfied for the calibration tones also.

From the above frequency response data, the gain balance of each channel can also be plotted. The requirement was for the fore and aft gains to be balanced in magnitude to within +/- 1.0 dB throughout the signal bandwidth. This response is plotted in Figure 3.2.6. What is required of the circuit is for the gain and the phase of the X and Y signal paths to track with frequency in the front-end bandpass amplifiers, and for the gains of the I and Q signals to

be matched throughout the chirp multiplication circuits and the CZT signal extraction circuits. The results show signal gain balance within +/- 0.1 dB. (How about that!)

Since the NASA scatterometers receive signals from both the fore and aft sectors, both up and down doppler spectra appear in the signal return. The Doppler discriminator must separate the fore and aft spectral data to assure isolation between the returns. The next tests were conducted to demonstrate that sufficient isolation exists between the fore and aft spectrum, the requirement set at greater than 30 dB. To test for fore/aft isolation, or separation between the quadrature channel paths, the input signal source setup was changed. The X and Y inputs of each channel were separated and sent quadrature signals of equal magnitude, that differed in phase by a variable amount around 90 degrees. The Y input lagged the X input. A representative response spectrum is shown in Figure 3.2.7, and it can be seen how the signal in the fore spectrum differs by more than 34 dB from the signal in the aft spectrum. This figure was with the source signals different in phase by 90.0 degrees, and balanced in magnitude to +/- 0.1 dB by measurement with the H-P gain phase meter. As the phase difference was changed to each side of -90 degrees, the responses were recorded and the tabulated results are plotted in Figure 3.2.8.

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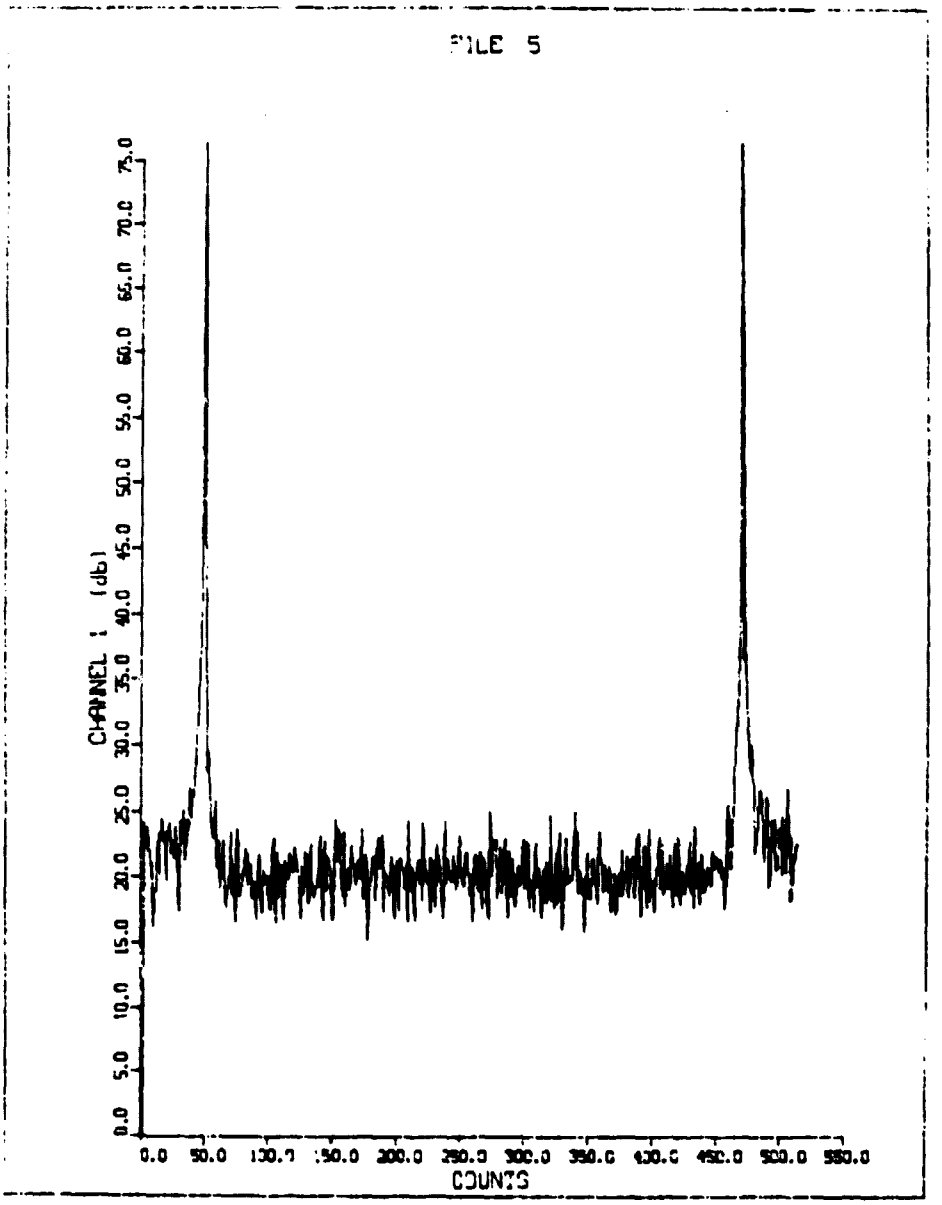

C-BAND

FIGURE 3.2.1 SPECTRAL PLOT, C-BAND, HIGH MAGNITUDE INPUT

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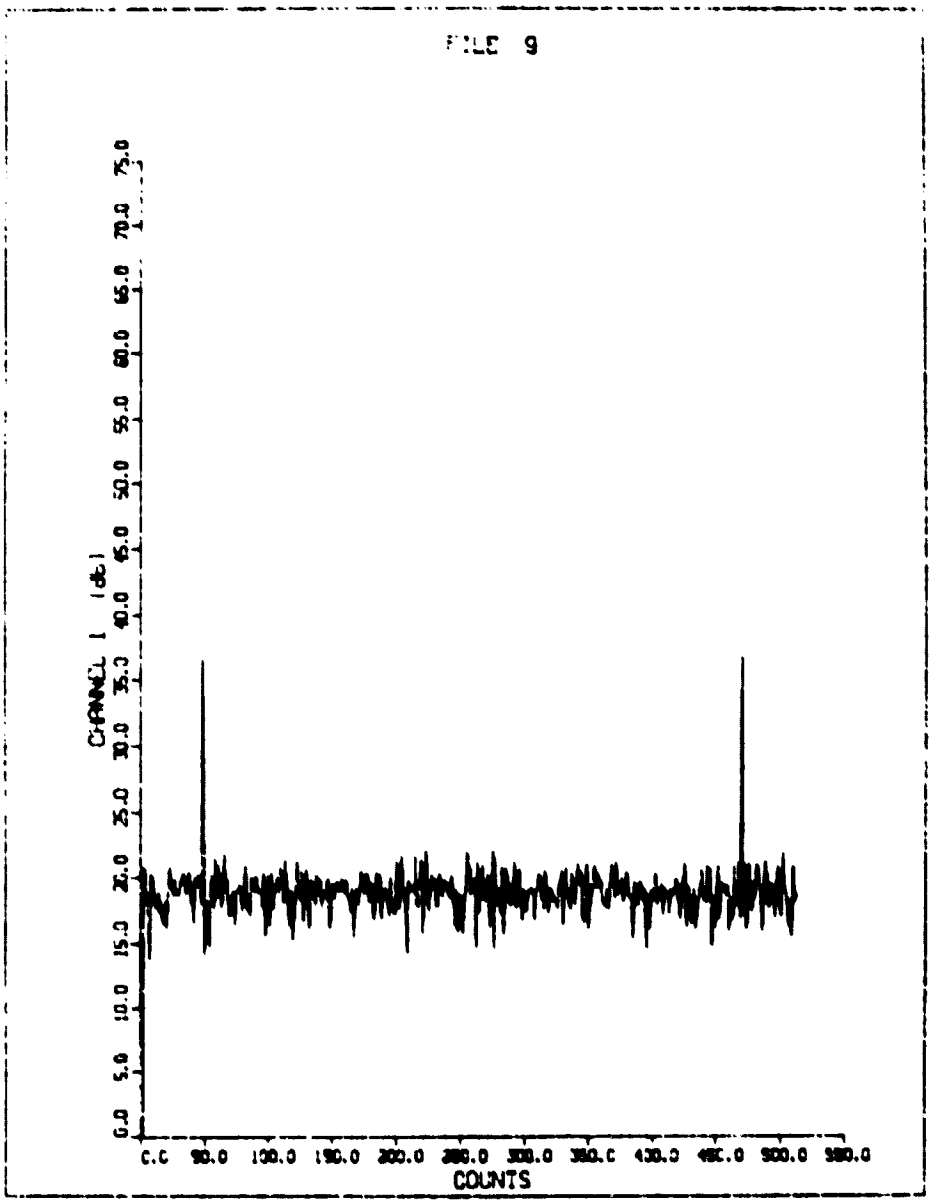

FIGURE 3.2.2 SPECTRAL PLOT, C-BAND, LOW-MAGNITURE INPUT

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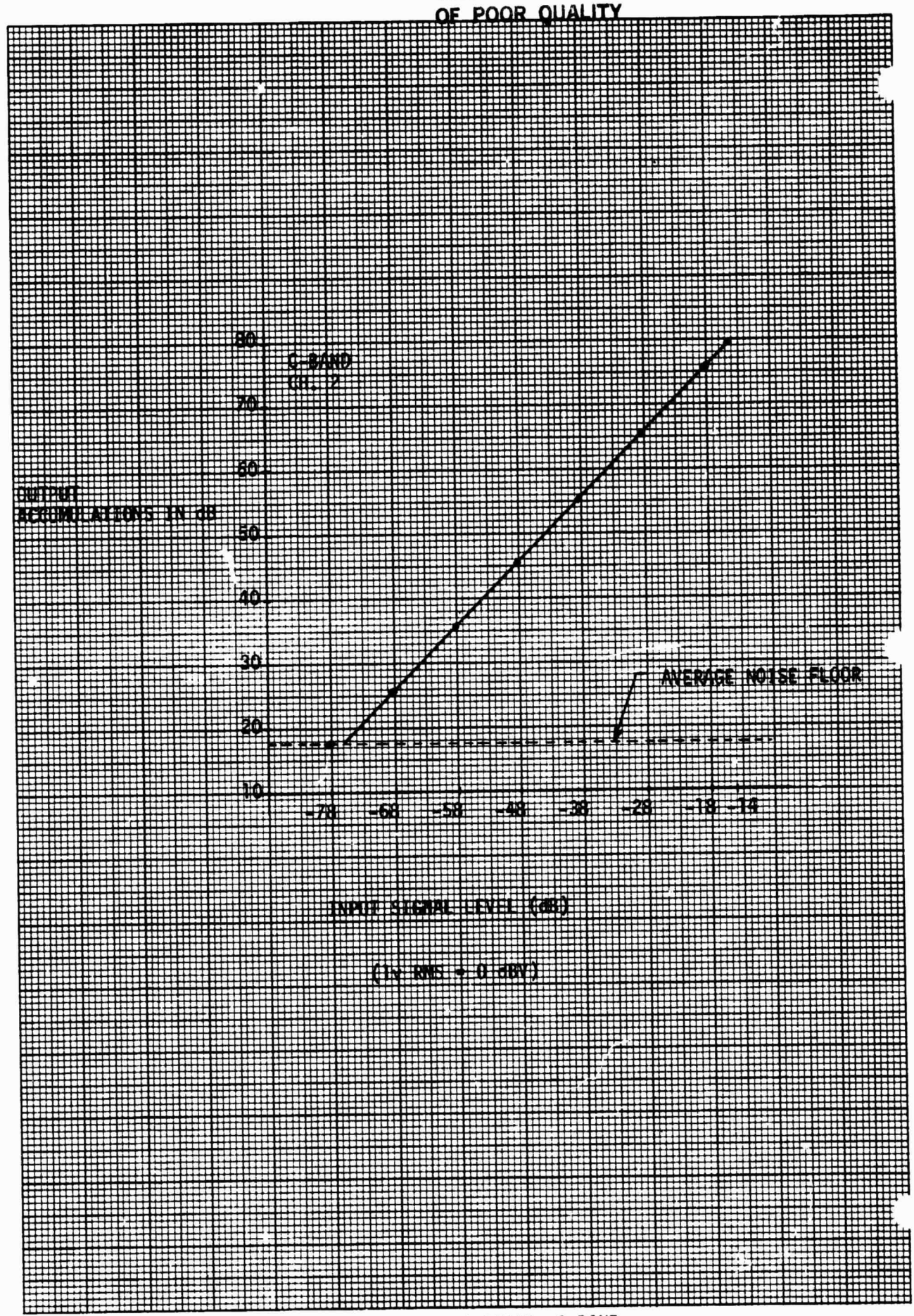

FF LOW 20 X 20 TO 1 INCH
SIX 10TH AND 20TH LINE PROGRESSIVELY ACCENTED

FIGURE 3.2.3 DYNAMIC RANGE, C-BAND

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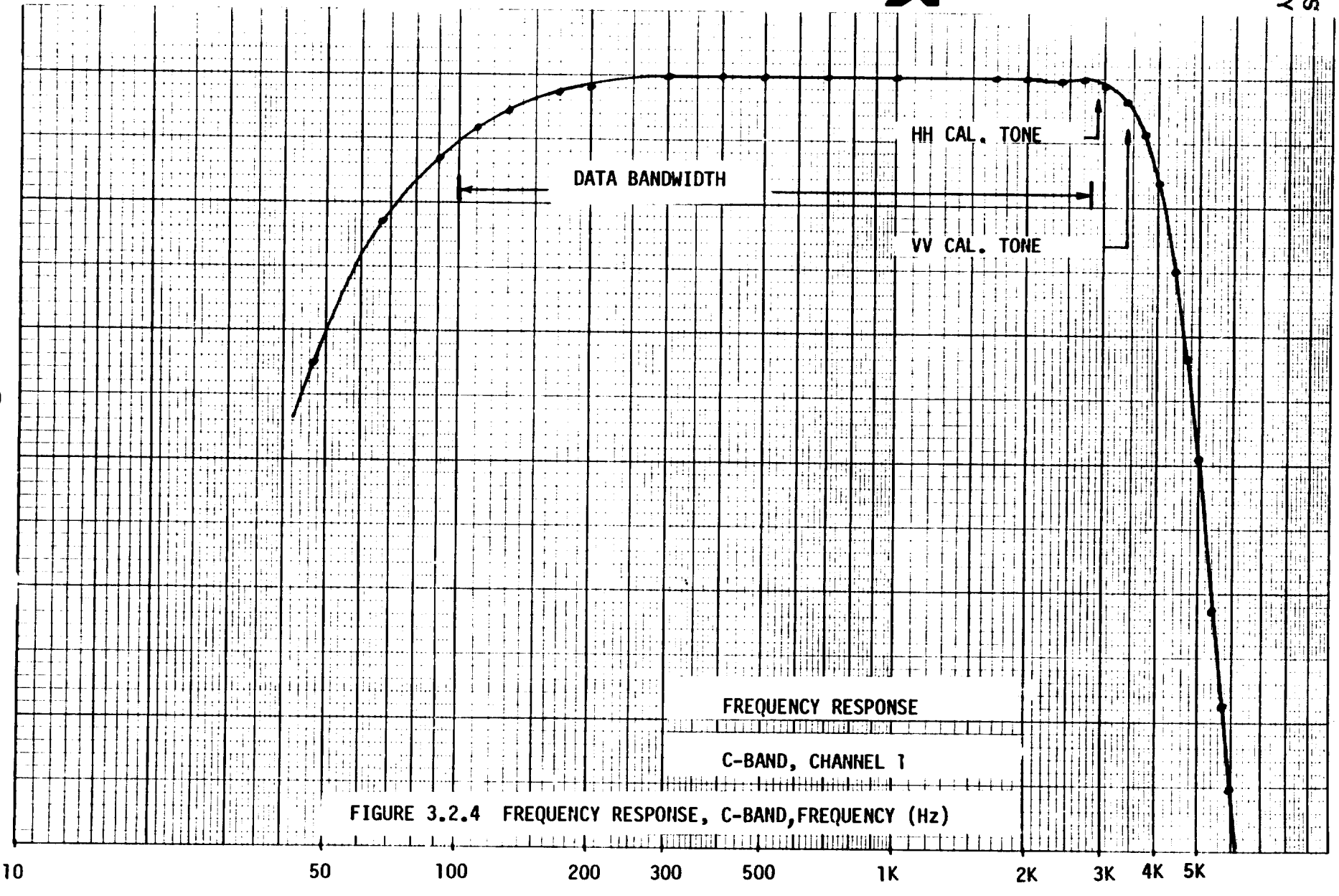

FIGURE 3.2.4 FREQUENCY RESPONSE, C-BAND, FREQUENCY (Hz)

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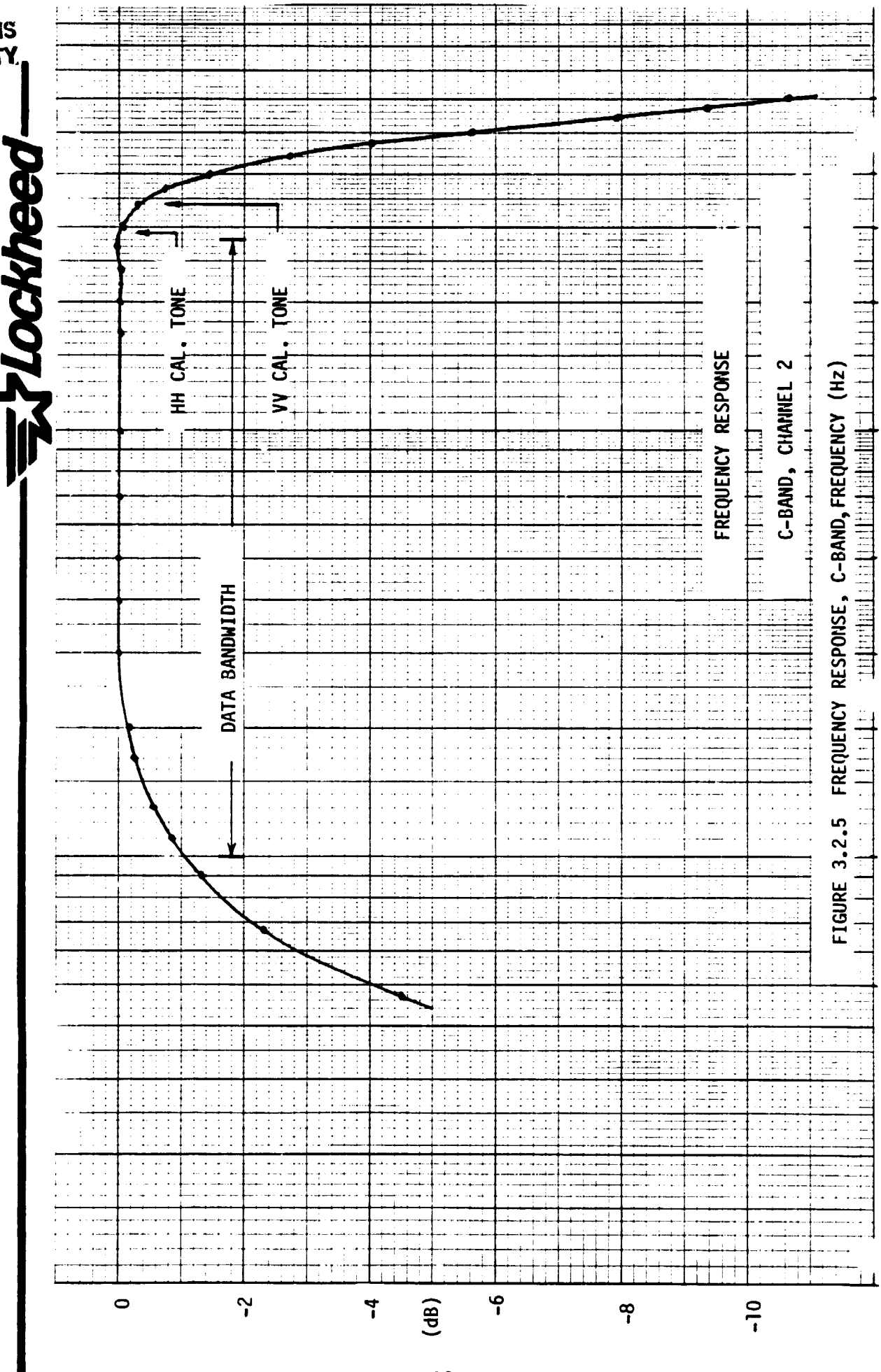

FIGURE 3.2.5 FREQUENCY RESPONSE, C-BAND, FREQUENCY (Hz)

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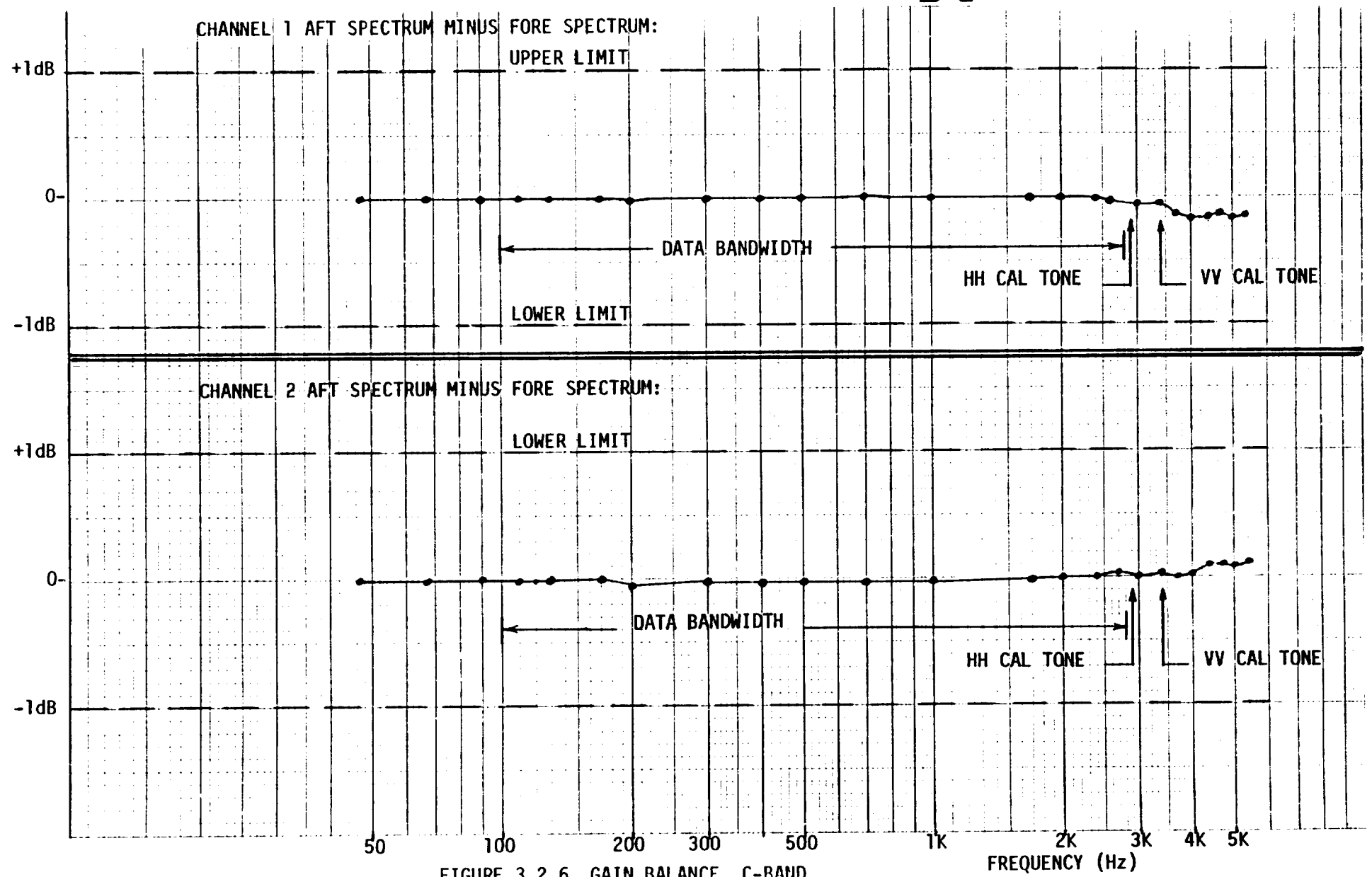

FIGURE 3.2.6 GAIN BALANCE, C-BAND

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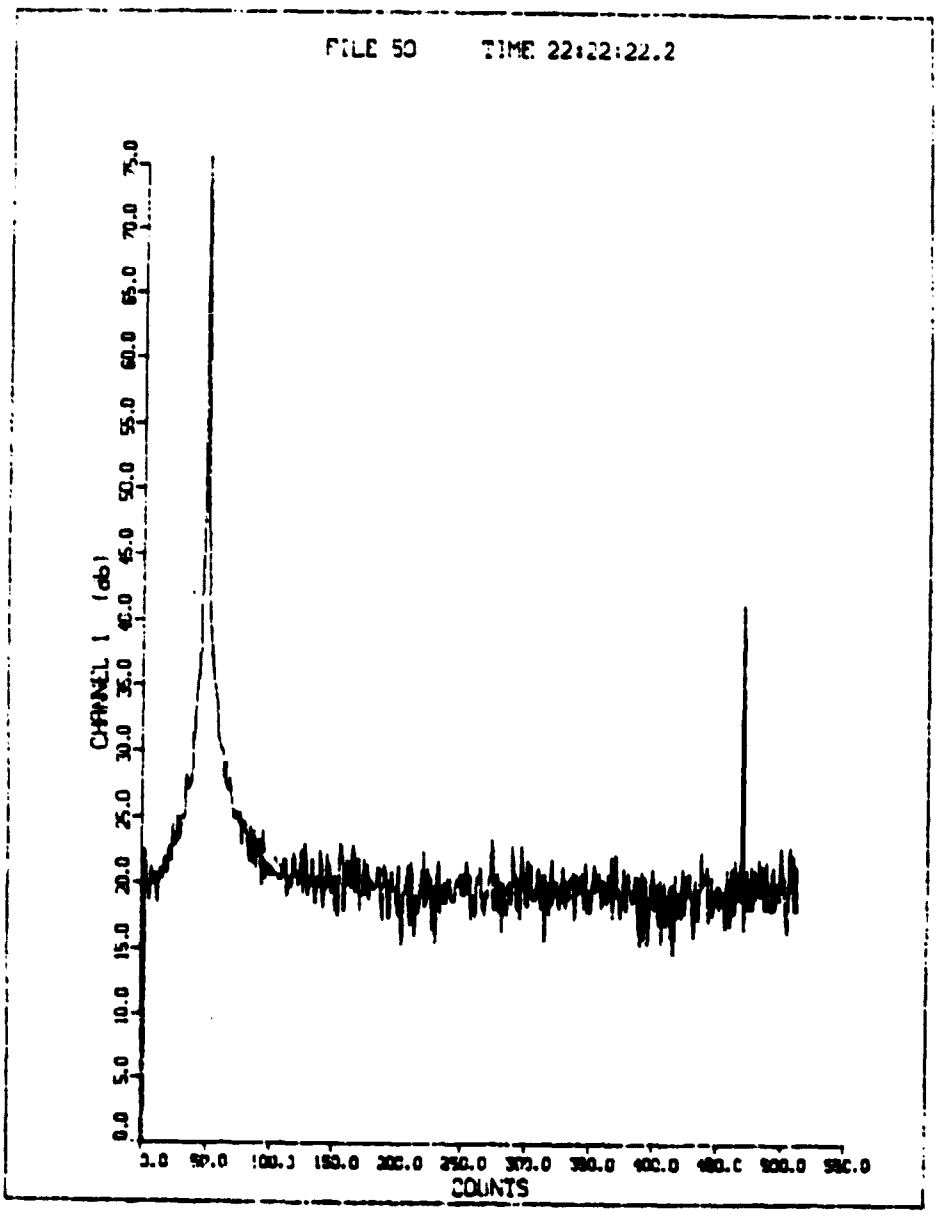

FIGURE 3.2.7 SPECTRAL PLOT, C-BAND, FORE/AFT ISOLATION

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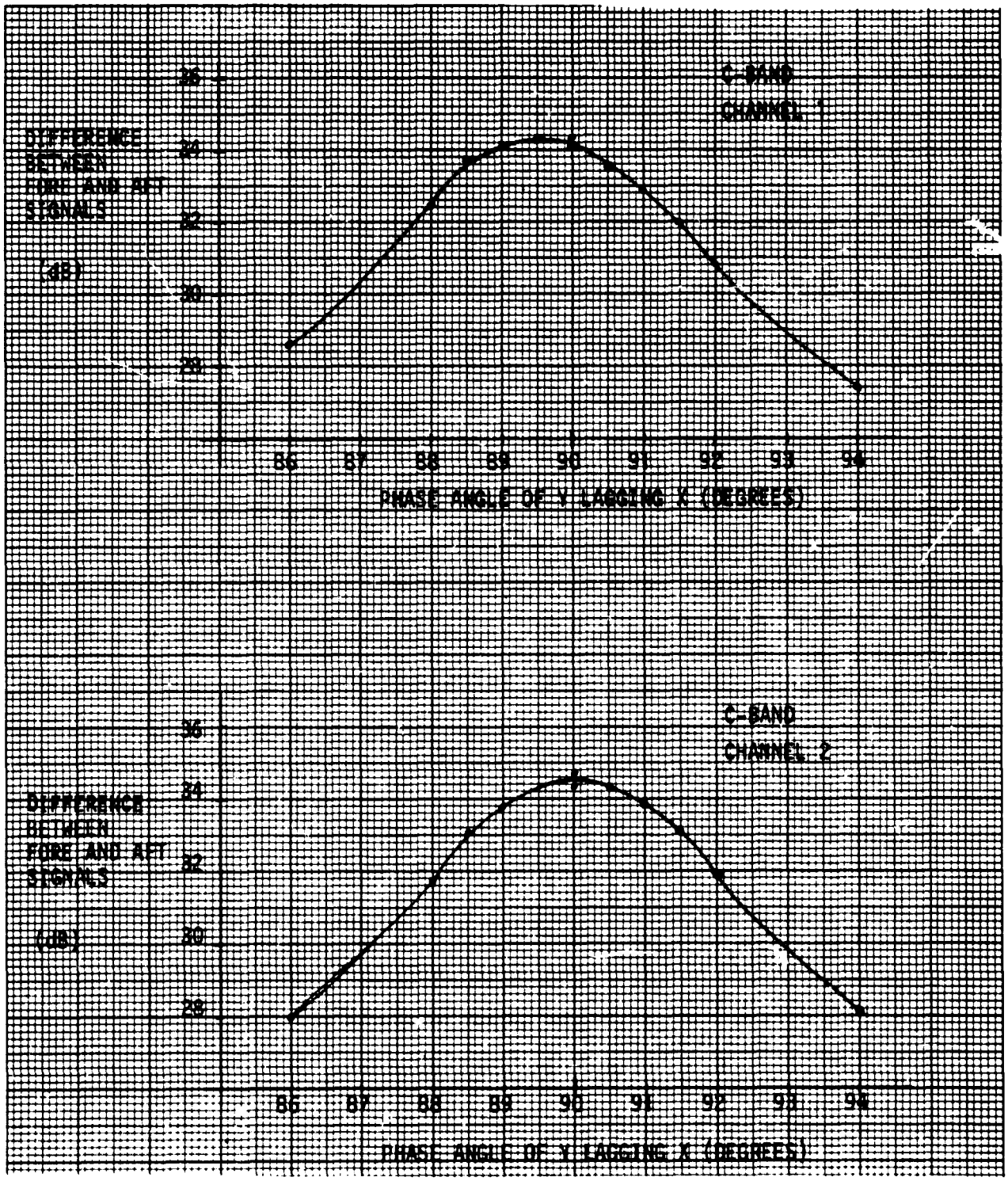

FIGURE 3.2.8 FORE/AFT ISOLATION PLOT

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The maximum separation occurs within +/- 0.5 degrees of -90.0 degrees and is well within the required range of +/- 2.0 degrees for phase balance for both data channels. The analog processors ability to meet this isolation, or separation between the fore and aft spectrum is largely a matter of properly balancing the gains in the quadrature channels at all data frequencies.

3.3 DISCUSSION OF L-BAND TESTS AND RESULTS

The same tests were run on the L-band processor with the exception of signal bandwidth. The first test run was for dynamic range and linearity, and both channels were tested together. The data that was taped performed its normal accumulation of 5 frames of analog PSD data for the intended one-half second averages. Typical spectral plots are shown in Figure 3.3.1 for a large input signal, and in Figure 3.3.2 for a lower signal level at 40 dB below the first figure. A plot of dynamic range and linearity results from the converted data is shown in Figure 3.3.3, where, similarily to the C-band data, the peak spectral amplitudes in dB were correlated with the input signals also measured in dB. From the plot, it is apparent that this system also exhibits a linear power-in to power-out relationship over a greater than 60 dB dynamic range.

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The frequency response tests were recorded and the tabulated data is plotted in Figures 3.3.4 and 3.3.5 for channels 1 and 2. The L-band scatterometer signal bandwidth is from 30 Hz to 1000 Hz, and the calibration tone is at 1900 Hz. Other polarization tones above 1900 Hz do exist in the L-band scatterometer data, but they are less than one-half the data sampling rate, or 2.60 KHz. The ripple across the input filter was not to exceed +/- 0.5 dB over the data bandwidth, and this requirement was satisfied. Note that the calibration tones at 1.9 KHz are attenuated by different amounts between the two data channels. This is due to the band pass filter characteristics being slightly different between the two channels, and therefore in the sigma-zero computations accomplished during ground data conversion, this difference may need to be taken into account.

From the above frequency response data, the gain balance of each channel can also be plotted, and is shown in Figure 3.3.6. The requirement was for the fore and aft gain to be balanced in magnitude to within +/- 1.0 dB throughout the signal bandwidth. As can be seen from the plot, the balance is well within the design limits in both channels, at about +/- 0.1 dB.

The last test was conducted to demonstrate the isolation between the fore and aft spectrum as described

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in the C-band tests and results with the input signals separated in phase by 90 degrees. A representative response spectrum is shown in Figure 3.3.7, and it can be seen how the signal in the fore spectrum differs by more than 35 dB from the signal in the aft spectrum. As the phase difference was changed to each side of -90.0 degrees, the responses were recorded and the tabulated results were plotted in Figure 3.3.8. The maximum separation occurs within +/- 0.5 degrees of -90.0 degrees and is also well within the required range of +/- 2.0 degrees for phase balance for both data channels. Recall that the analog processors ability to meet the isolation and gain balance between fore and aft spectrums is largely a matter of properly balancing the gains in the quadrature channels at all data frequencies.

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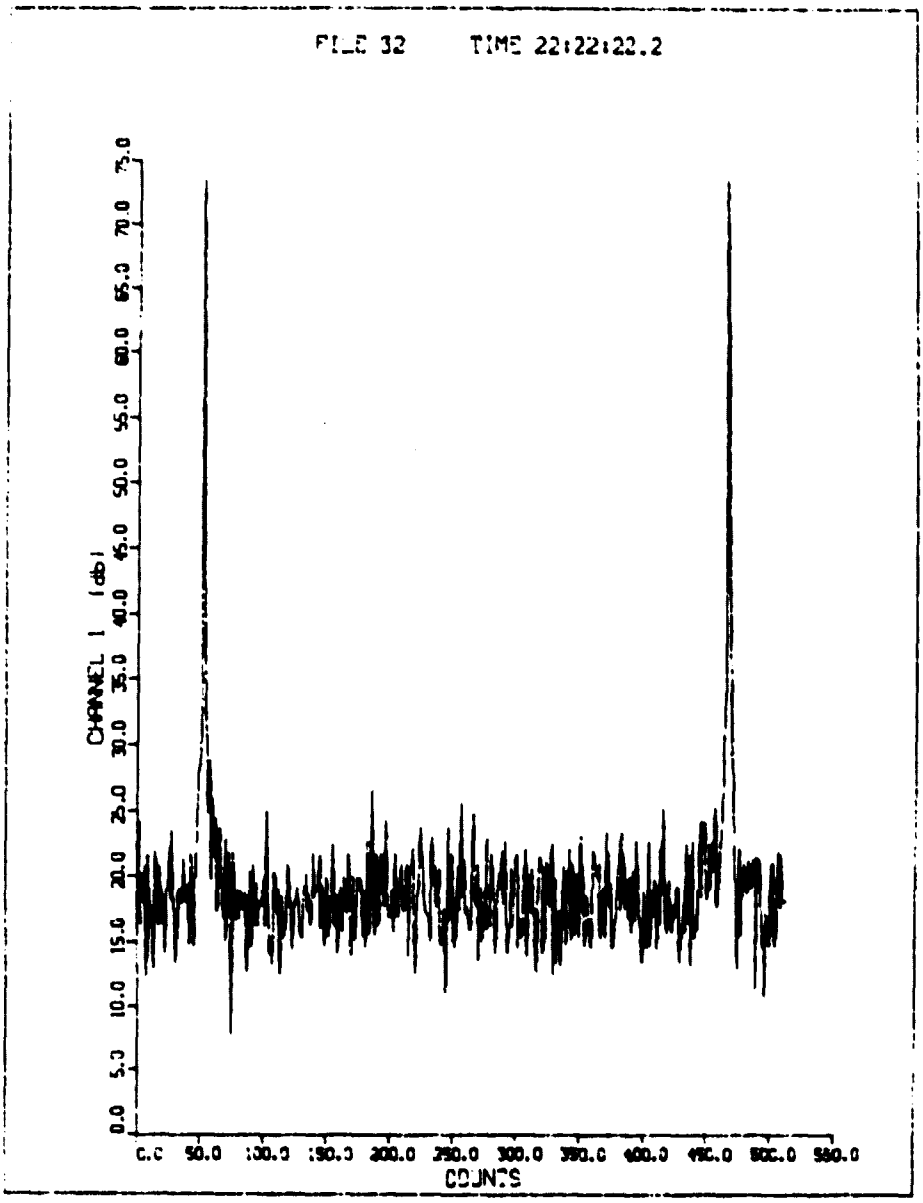

FIGURE 3.3.1 SPECTRAL PLOT, L-BAND, HIGH MAGNITUDE INPUT

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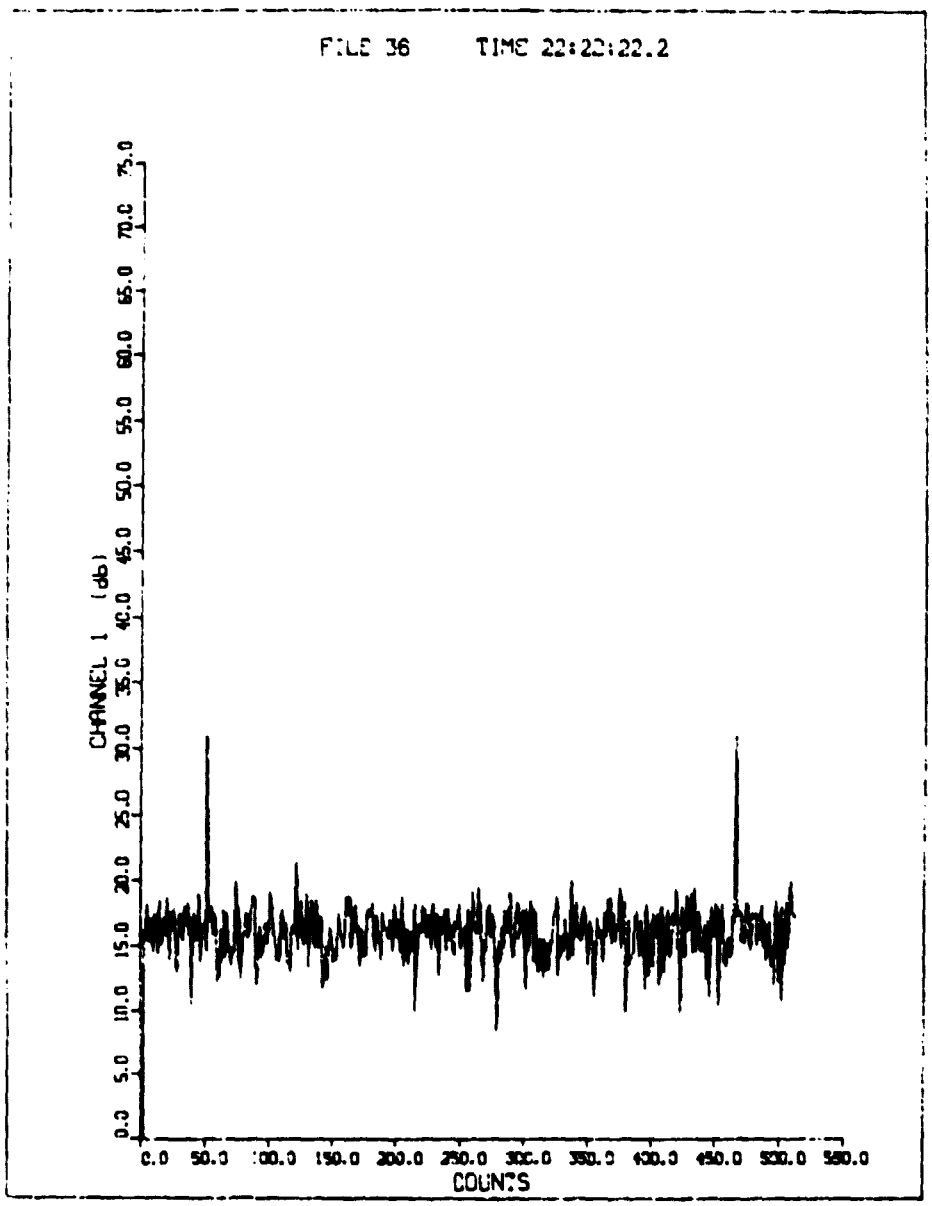

FIGURE 3.3.2 SPECTRAL PLOT, L-BAND, LOW MAGNITUDE INPUT

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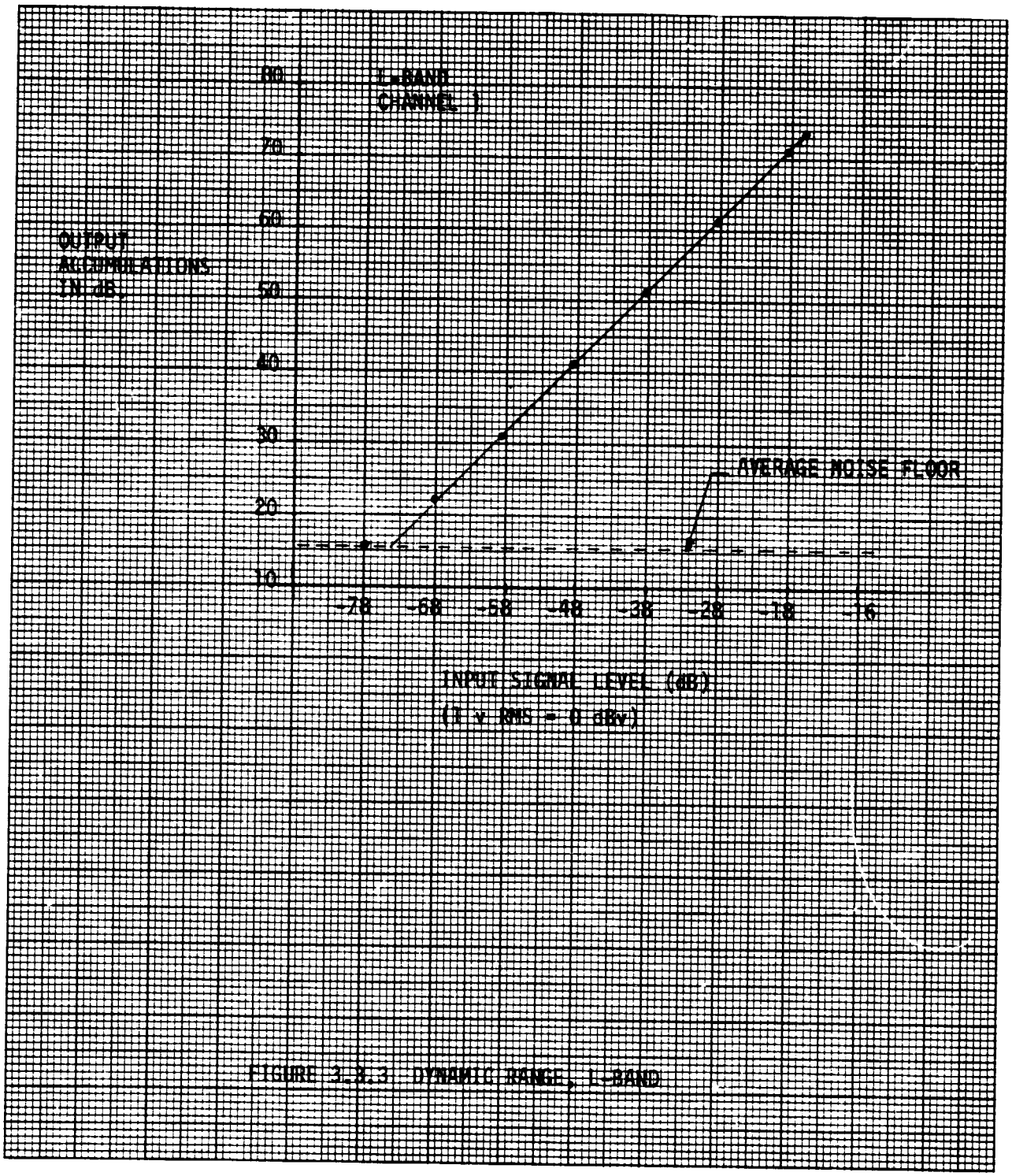

FIGURE 3.3.3 DYNAMIC RANGE, L-BAND

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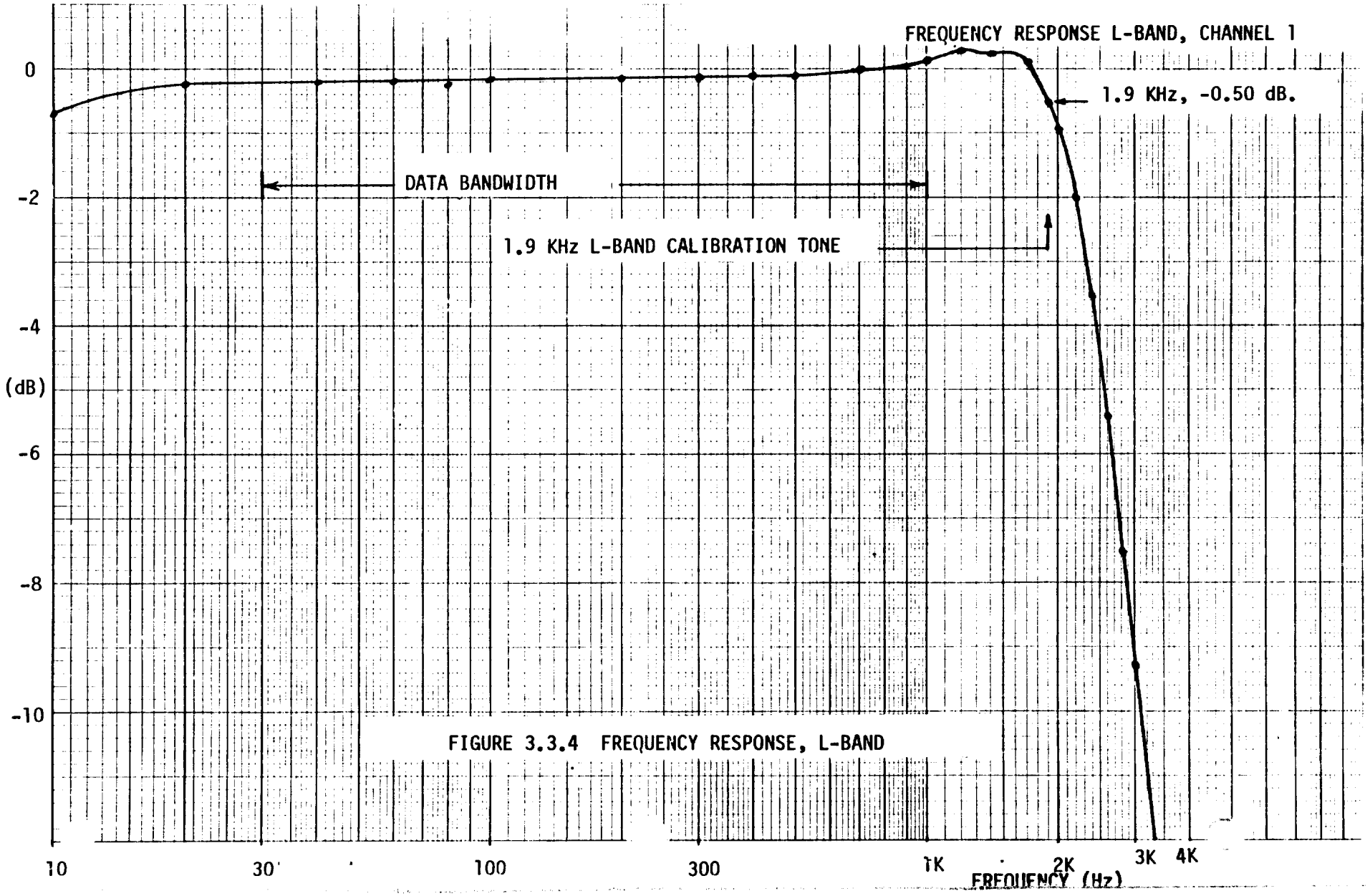

FIGURE 3.3.4 FREQUENCY RESPONSE, L-BAND

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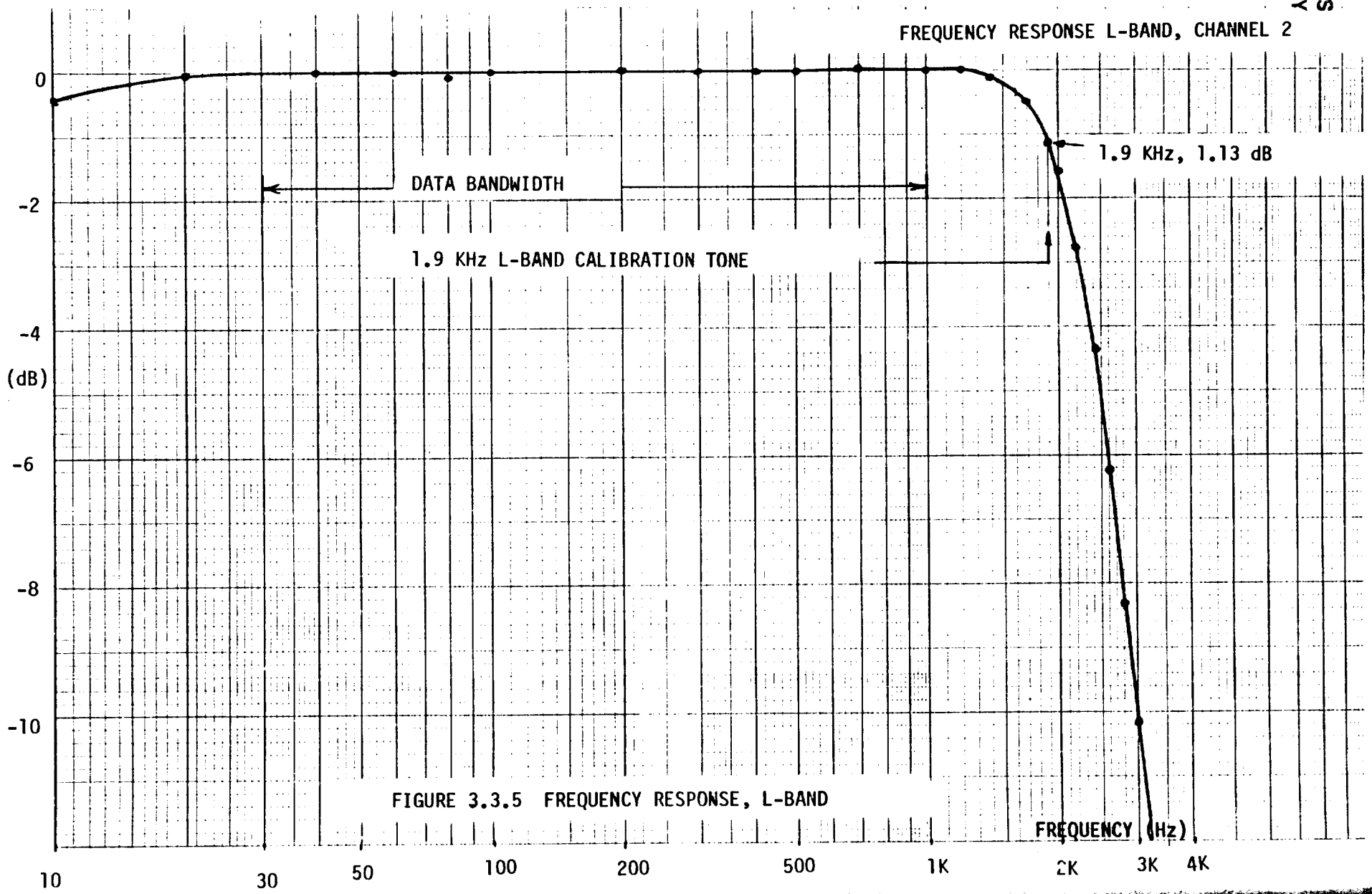

FIGURE 3.3.5 FREQUENCY RESPONSE, L-BAND

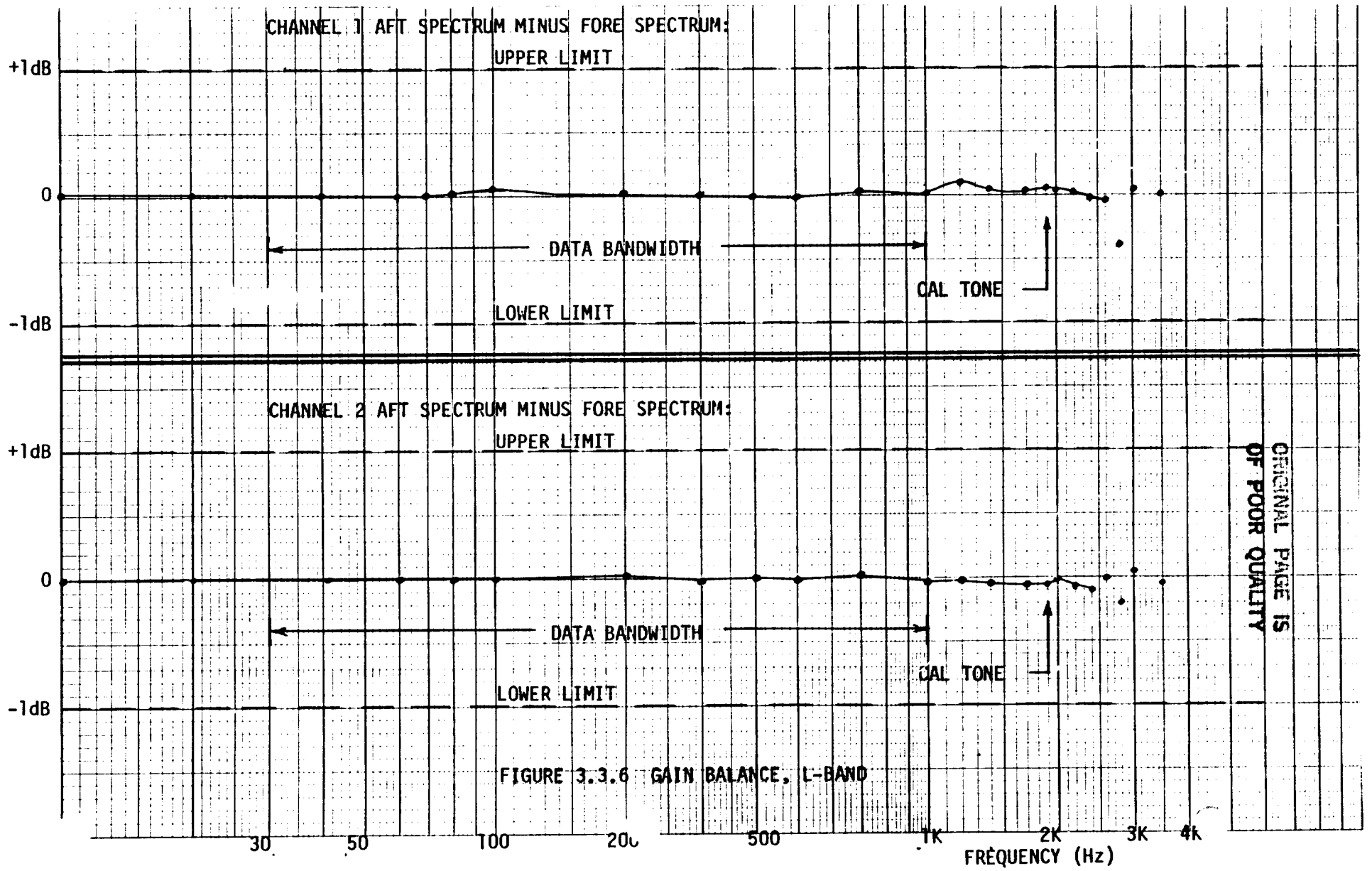

FIGURE 3.3.6 GAIN BALANCE, L-BAND

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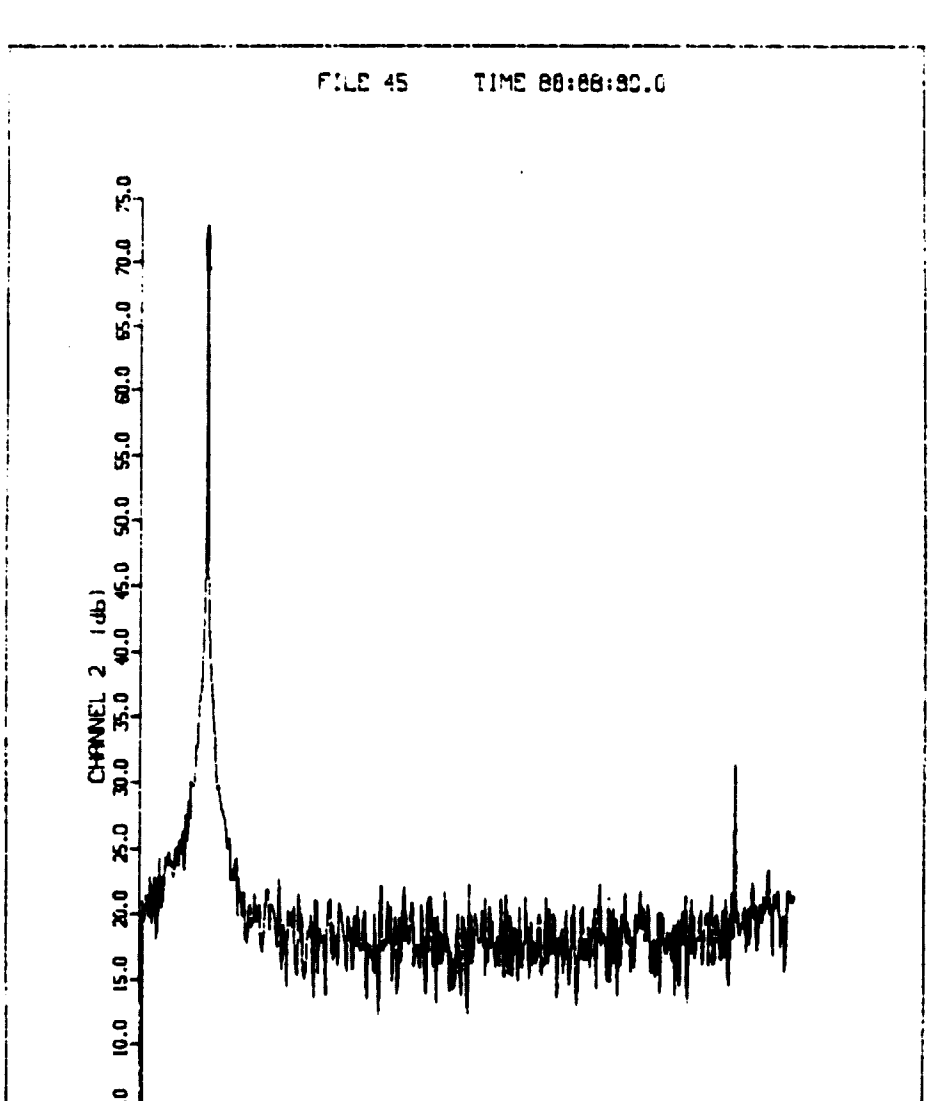

FIGURE 3.3.7 SPECTRAL PLOT, L-BAND, FORE/AFT ISOLATION

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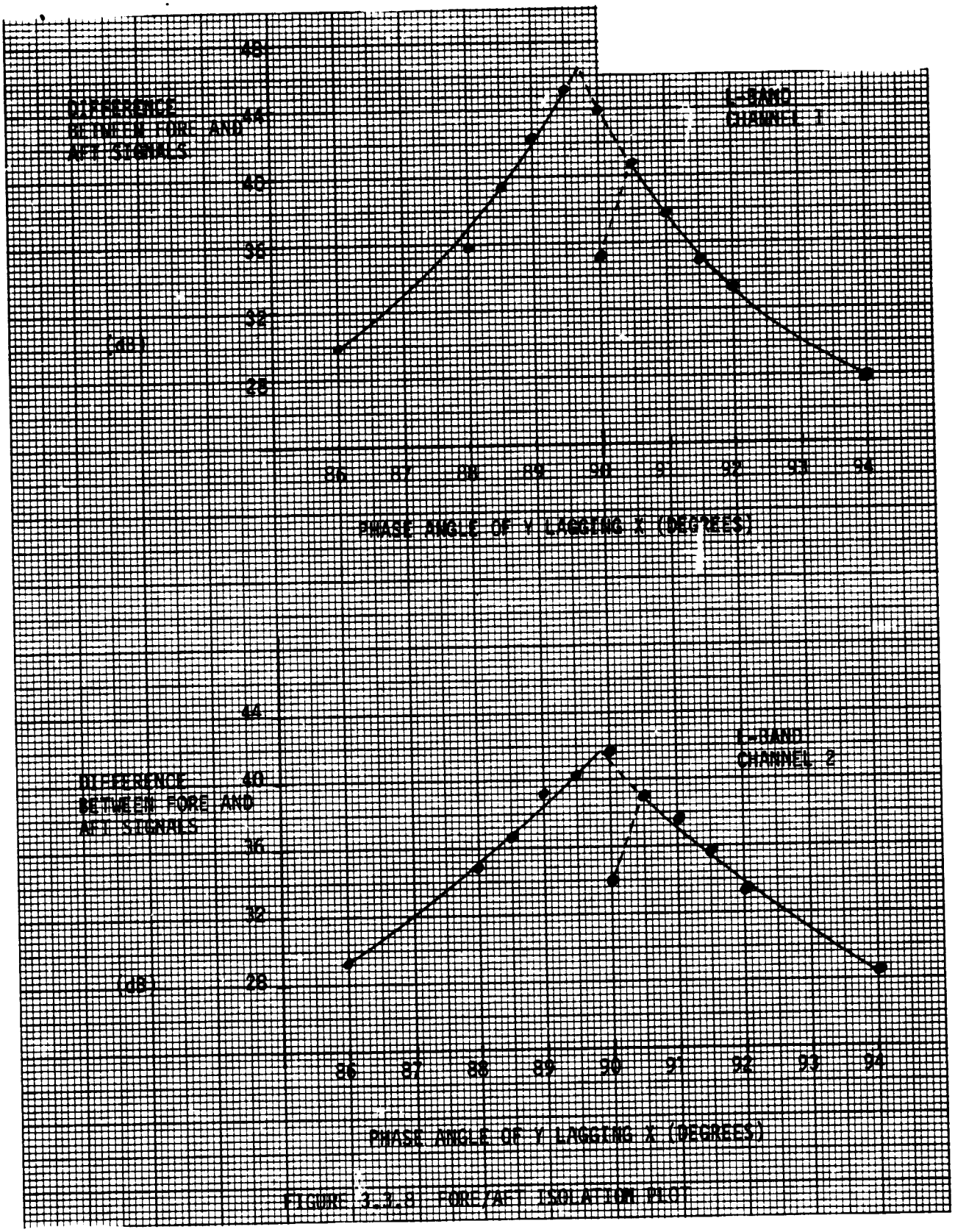

FIGURE 3.1.8 FORE/AFT ISOLATION PLOT

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3.4 TEST RESULTS FROM RECORDED FLIGHT SCATTEROMETER DATA

The L-band and C-band PSD processors were operated in the SAL lab with input data from a previously flown functional check flight (FCF) test tape. The flight tape data tracks are marked Like-Sine, Like-Cosine, Cross-Sine, and Cross-Cosine. These correspond to the PSD processors inputs marked Channel 1-X Input, Channel 1-Y Input, Channel 2-X Input, and Channel 2-Y Input.

Frequency spectrum plots of two different C-band frames and two different L-band frames are shown in Figures 3.4.1a and .1b, and Figures 3.4.2a and .2b. The C-band calibration/polarization tone appears in the fore spectrum as it should, and the aft spectrum has a higher level of return than the fore spectrum, since the antenna beam is directed primarily aft. The other spikes that are symmetrical in the fore and aft spectrum were suggested as being noise spikes by a sensor engineer. Note how much the noise floor has been raised from the lab test data, but recall that this data was being played back from an instrumentation tape recording.

The L-band data shows the 1.9 kHz calibration tone and a polarization tone at a slightly higher frequency, and both are symmetrical in the fore and aft spectrums.

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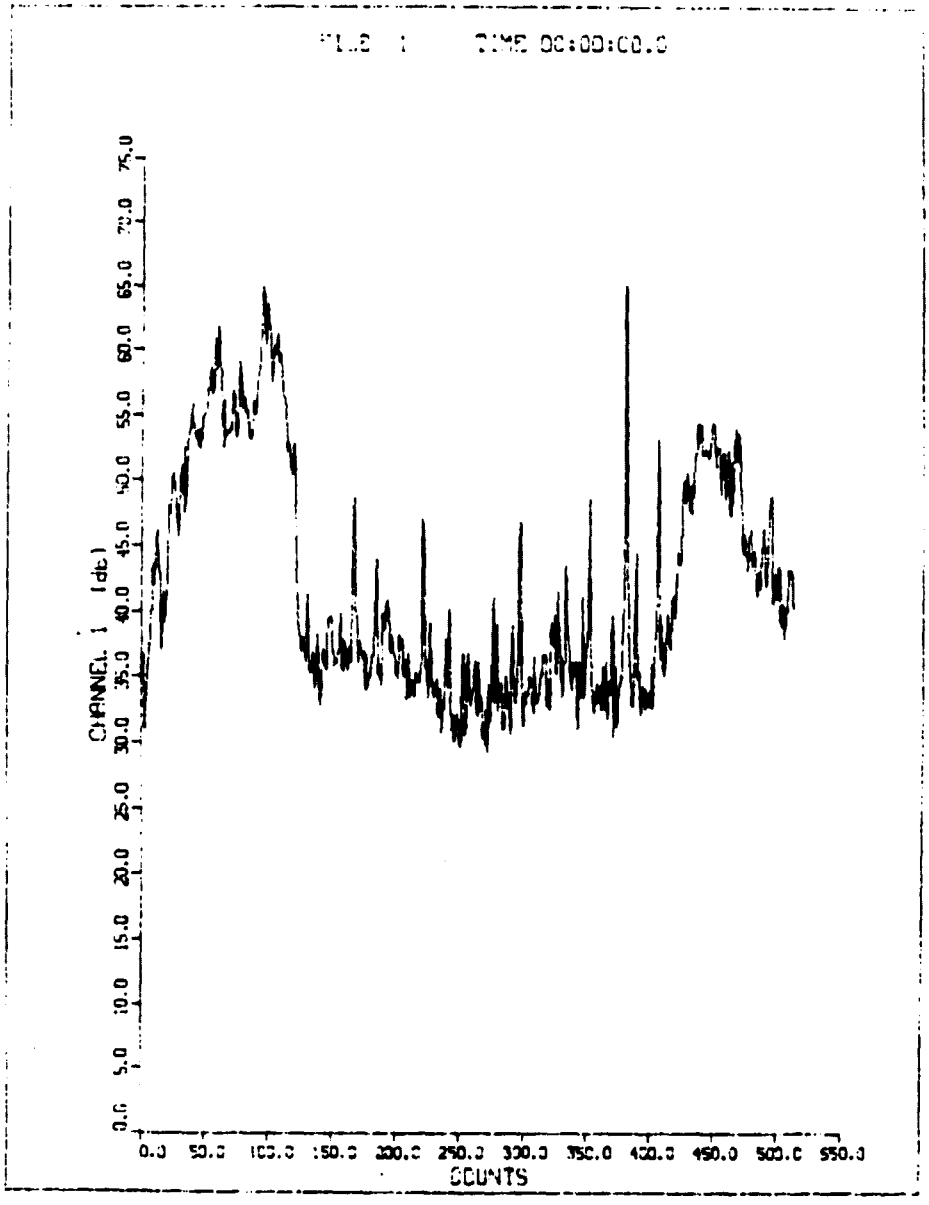

FIGURE 3.4.1(a) SPECTRAL PLOT OF C-BAND FLIGHT DATA

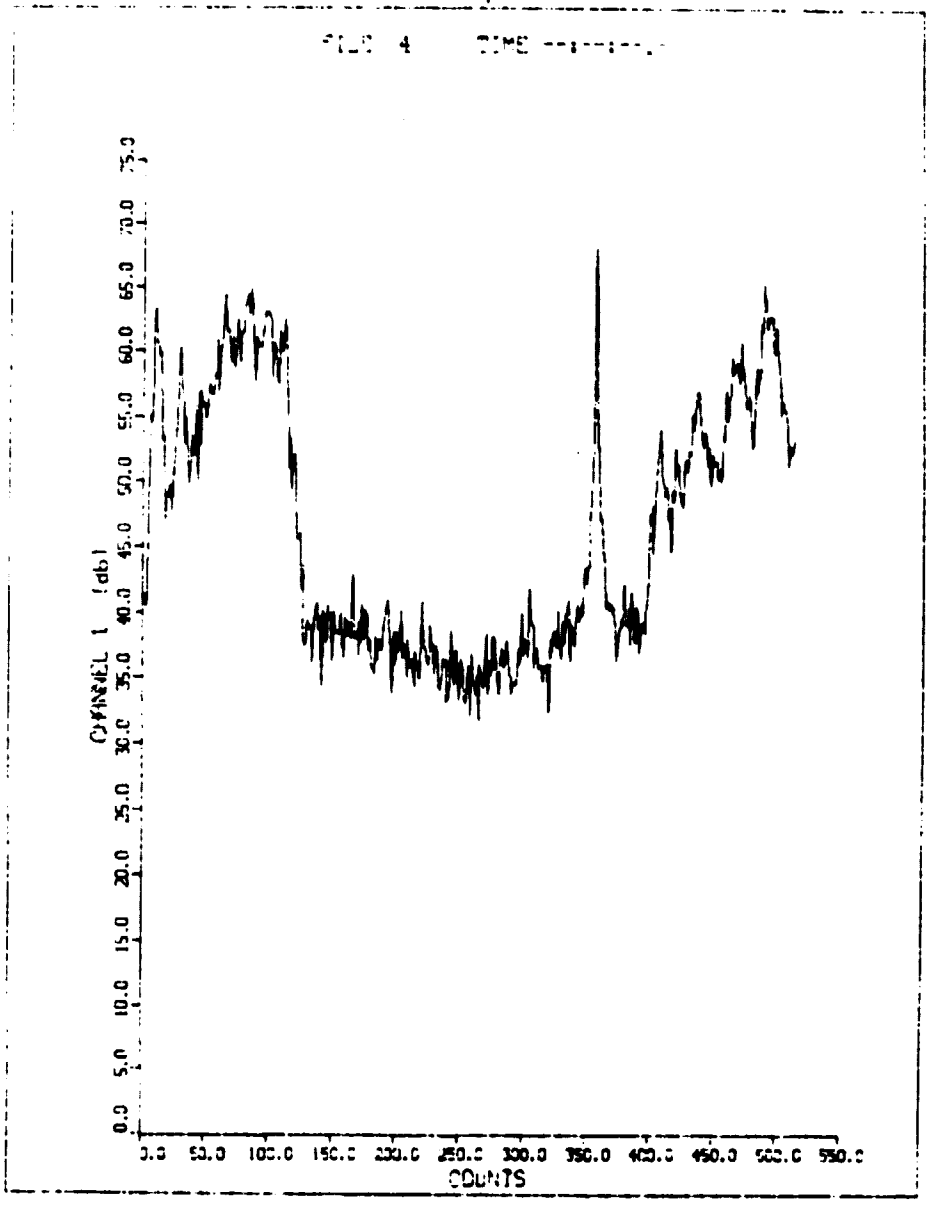

FIGURE 3.4.1(b) SPECTRAL PLOT OF C-BAND FLIGHT DATA

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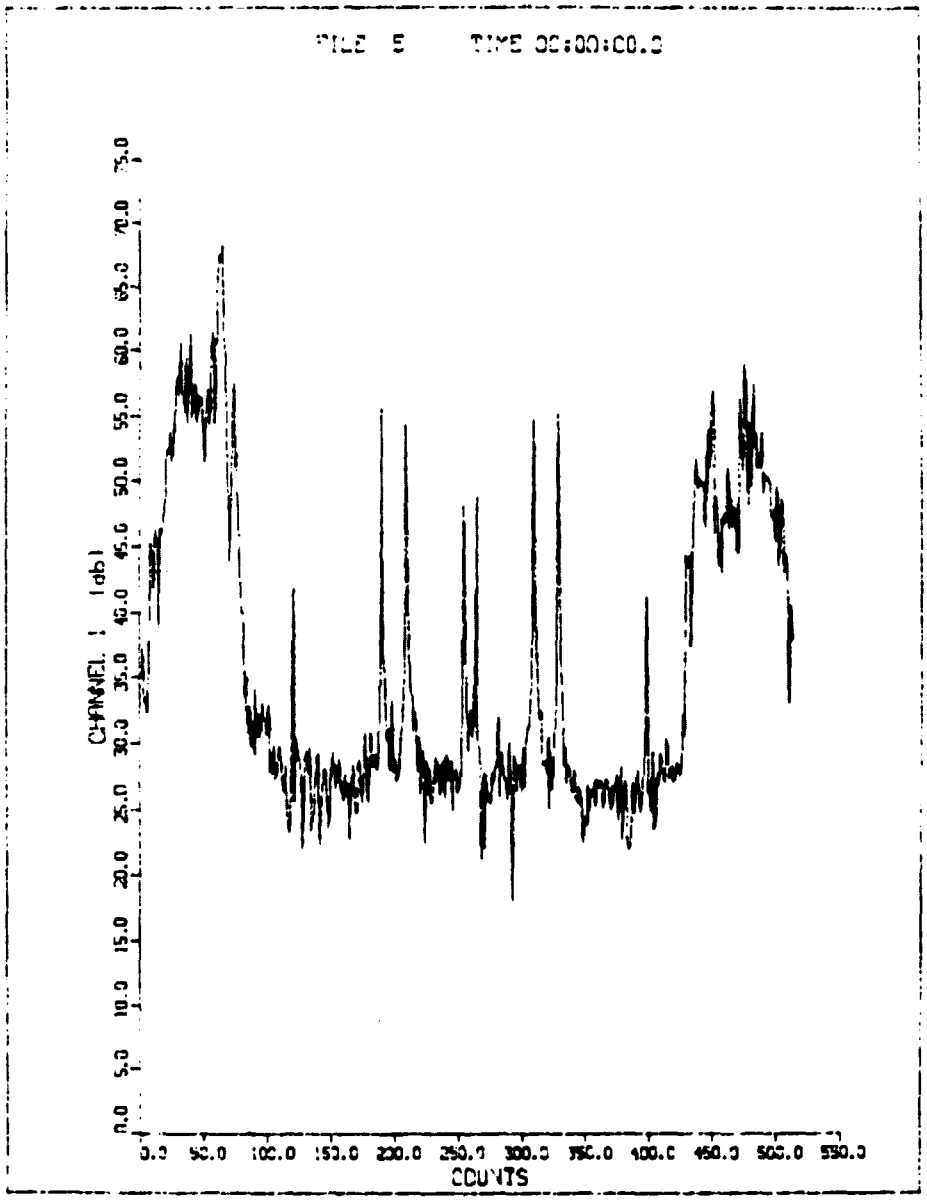

FIGURE 3.4.2(a) SPECTRAL PLOT OF L-BAND FLIGHT DATA

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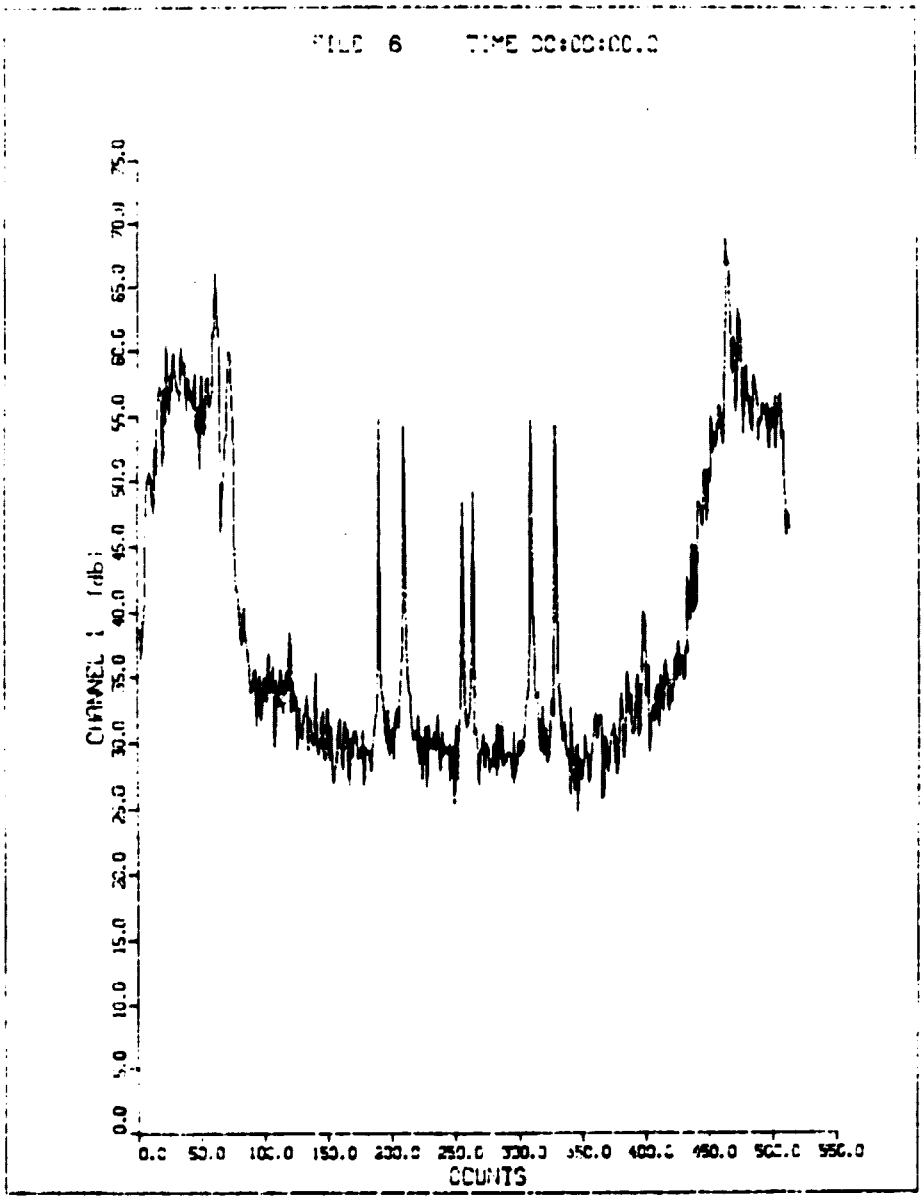

FIGURE 3.4.2(b) SPECTRAL PLOT OF L-BAND FLIGHT DATA

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The additional symmetrical spikes were also suggested as being antenna cable and/or connector problems.

3.5 GENERAL DISCUSSIONS OVER TEST RESULTS

The overall performance of the two PSD processors was considered to be very good in meeting or surpassing all design goals. There were only a couple of test results that warrant discussion, and one result that warrants operational consideration.

The only anomalies in the C-band tests were in the low frequency rolloff and in the phase balance test. As was noted in the frequency response envelope in Figures 3.2.4 and 3.2.5, the bandpass characteristics begin to rolloff within the data bandwidth, but do stay within the requested +/- 0.5 dB. If determined by the user of the equipment, this low frequency response may want to be altered. The only other questionable result was in the phase balance test plot of Figure 3.2.8. It was noticed that the magnitude of the difference between aft and fore signals was not as great in the C-band channels as it was in the L-band channels.

The only anomalies in the L-band tests were in the high frequency peaking in channel 1 and in the phase balance results. As was noted in Figures 3.3.4 and 3.3.5, the bandpass characteristics of channel 1 has

amplitude peaking just prior to the high frequency rolloff of approximately +0.4 dB over the midband gain, whereas all the other channels have much flatter frequency response characteristics. It still satisfies the design requirement of +/- 0.5 dB maximum ripple, but the users may wish it to be altered. Actually the only real anomalie occured in the phase balance test on the L-band channels. At the start of the test, the quadrature signals were set for -90.0 degrees, and for this data point only the result was considerably off the plotted curve shown in Figure 3.3.8. The test started at -90.0 degrees and went in steps to -94.0 degrees, then came back and repeated -90.0 degrees and finished in steps at -86.0 degrees. The test was not repeated after this was noticed in the data, and the only explaination offered is in the test setting.

Both systems have a characteristic that was observed from the analysis of the frequency response tests. When the high level input signals occured right around the Nyquist frequency of one-half the sampling rate, then there was a shift upwards in the level of the noise floor by as mush as 15 to 18 dB. As the input signal increased past the Nyquist frequency, the noise floor returned to the original level and the PSD signals crossed over between the fore and aft spectrums. The input bandpass filters are attenuating those higher frequency signals, but the filter rolloff frequency and

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the Nyquist frequency are not far apart. This is only a characteristic of the processor, and should not affect the scatterometer sensor data, since there should not be any signals of appreciable magnitude at or past the Nyquist frequency. However, as was noted from the recorded flight scatterometer data tape, there were significant noise spikes in the spectrum, expecially in the L-band data, that were stated as antenna and/or cable problems.

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4.0 ADDITIONAL DOCUMENTATION

In addition to this document, these items are provided:

1) Alignment procedures
2) Drawing list
3) Parts list.

4.1 Alignment Procedures

4.1.1 X and Y Gain Adjustment
(R3,R4; Ref. SIE 39115721, sheet 1)

Monitor the X and Y signal test points on connector P4. Equalize the signal magnitude at these outputs for a common input signal level (at a mid-band frequency). The X and Y output magnitude should be at least 1.5 volts ac, equal to within 1 mv.

4.1.2 X and Y Offset Adjustment
(R5 & R6: Ref. dwg. SIE 39115721, sheet 1)

Monitor the T&M board DAC output (available at the chassis backpanel). Select DAC for I squared (I^2) and Q squared (Q^2) outputs using DIP switch position 4 on the T&M Board. Remove any input signal. Using DIP switch position 2, monitor I^2 output for X offset adjustment, Q^2 output for Y offset adjustment. Adjust

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X (or Y) offset pot so PSD bin number three in the aft spectrum is the same average value as the noise floor. Bin number three is the location of the dc content of the PSD spectrum.

4.1.3 CZT Offset Adjustment

(R7 & R8: Ref. dwg. SIE 39115721, sheet 2)

Monitor the TP outputs of LH2201AD (U20-22) and adjust appropriate pot for a dc level of 5.25 volts with no input signals.

4.1.4 I and Q Offset Null Adjustment

(R9,R10: Ref. SIE 39115721, sheet 4)

(Refer to the last paragraph of section 2.2.2 for explaination of the test DAC circuit).

Install the Engineering T&M board in place of the flight board. Monitor the 8 bit Test DAC (ref. dwg. SIE 39115723, sheet3). Remove any input signals. Connect the first of the four MPLY lowest 8 bit or the voltage output of the Test DAC. Adjust that channels I (or Q) offset null pot (ref. dwg. SIE 39115721, sheet 4) for minimum output levels. Accomplish same on each channels I and Q signals. Replace the flight T&M Board. (NOTE: The X and Y offset adjustment in 4.1.2 could be more accurately set using this test DAC method.)

4.2 Drawing List

All schematics and board layouts on the Analog Subsystem of the PSD Processor are listed:

Drawing number		Drawing title
SIE 39115719		Block Diagram of Signal Conversion
SIE 39115720		Chassis Power Wiring
SIE 39115721	Sheet 1	Analog Board-Input Dual BPF Circuit
"	Sheet 2	" -MDAC and CZT Filter Circuit
"	Sheet 3	" -Sine & Cosine Chirp PROM Circuit
"	Sheet 4	" -CZT Extraction and ADC Circuit
"	Sheet 5	" -ADC Buffer and Decom Circuit
SIE 39115722		Analog CZT Board Layout
SIE 39115723	Sheet 1	Timing and Multiplier Board-Timing Circuit
"	Sheet 2	" -Multiplier Circuit
"	Sheet 3	" -Test DAC and Test Signal
SIE 39115724		Timing and Multiplier Board Layout
SIE 39115725	Sheet 1	Analog Subsystem Card Cage Wiring-J1 & I/O
"	Sheet 2	" -J2 & I/O
"	Sheet 3	" -J3 & I/O

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4.3 Parts List

4.3.1 Analog CZT Board Active Components

Part Number	I.C. Location	Source
LH2201AD	U3-1, U5-11, U20-22	National
LH2208AD	U3-21, U3-31, U34-51	National
LF347BN	U7-51, U20-9, U20-41, U30-33, U36-24	National
LF353AN	U3-41, U3-55	National
LF353BN	U7-31, U34-5	National
HI1-5043-5	U7-1, U1-11, U7-21	Harris
HI1-200-5	U3-47, U38-51	Harris
DAS-HS-12BM	U18-1, U18-11, U18-41, U18-51	Datel-Intersil
AD7541TD	U9-51, U36-10	Analog Devices
D2708-2	U11-12, U11-30, U11-48	Intel
DS0026CN	U26-11, U26-16, U30-11, U30-16	National
R5601-1	U28-21	Reticon
AD583KD (*)	U38-32, U38-41, U28-42	Analog Devices
	(*)Alternates: SHM-IC-1	Datel-Intersil
	HA1-2420-5	Harris
ADC-HS-12BM	U43-21, U43-41	Datel-Intersil
SN7404N	U41-1, U43-1, U45-1, U43-11, U45-11	T.I.
SN74LS298N	U39-1, U39-11, U41-11	T.I.
1N825	D1, D2, D3	
1N746A	D4	
1N916	D5, D6, D7	
1N751A	D8	

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1N759A	:	D9
AD589KH	:	D10, D11

Analog Devices

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4.3.2 Timing and Multiplier Board Active Components

Part Number	I.C. Location	Source
SN74LS193N	U1-1, U3-11, U3-21, U10-1, U10-11	
SN7400N	U1-11	
SR74-1, 5.0 MHz	U1-21	Connor-Winfield
D2708-2	U5-1, U5-17	Intel
SN74174N	U8-1, U8-11, U8-21	
SN7474N	U10-21	
SN7425N	U12-1	
SN7420N	U12-11	
SN7404N	U12-21	
ICL8038BMJD	U10-31	Intersil
MPY-12HJ	U18-1, U28-1, U34-1, U44-1	TRW
SN74283N	U22-11, U24-11, U24-21, U22-31, U22-41, U22-51, U38-11, U40-11, U40-21, U38-31, U38-41, U38-51	
SN74LS157N	U26-11, U24-31, U24-41, U24-51, U42-11, U40-31, U40-41, U40-51	
SN74LS158N	U26-21, U26-31, U26-41, U26-51, U42-21, U42-31, U42-41, U42-51	
DAC-HP-16BMR	U28-37, U44-37	Datel-Intersil
LF353BN	U28-56, U44-56	National
1N751A	D1	
1N759A	D2	

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4.3.3 Passive Components

Resistors:

* All resistors called out to three place values are 1% metal film type RN55D.
* All other unspecified resistors are 5% carbon, 1/4 watt, type RCR07.
* All specified 1/2 watt resistors are 5% carbon, type RCR20.

Potentiometers: (Bourns or equivalent)

R3 and R4	P/N 3299W1-103, 10K	Gain pots for X and Y
R5 and R6	" " "	Offset pots for X and Y
R7 and R8	" 3299W1-102, 1K	CZT offset pots
R9 and 10	" 3299W1-103, 10K	Offset null pots I and Q

Switches:

* All switches on the cards are four position DIP (dual-inline-package) such as C&K model BD04, or equivalent.

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Capacitors:

* All power supply bypass capacitors labeled 0.1 uf on the schematic drawings are ceramic p/n 3CZ5U104XD050C5 in the analog circuits and AVX p/n MD015C104KAA in the digital circuits.
* Balance of capacitors are listed:

Analog CZT Board (ref. dwg. SIE39115721):

Component No.	Value	Part No.	Source
C1 thru C12	See Schematic, sheet 1: BPF		Kemet, C320xxxK2G5CA
C13 thru C20	33 pf	C320C330K2G5CA	"
C21, C22	1800 pf	B6A182J	Elpac
C23, C24, C25	15 uf	CSR13E156KS	
C26 thru C32,	5.6 uf	CSR13E565KS	
C58, C59,	"	"	
C81 thru C84	"	"	
C33 thru C36	560 pf	C320C561K2G5CA	Kemet
C37 thru C40	82 pf	C320C820K2G5CA	"
C41, C42, C92	10 pf	C320C100K2G5CA	"
C43 thru C50	470 pf	C320C471K2G5CA	"
C51 thru C56	1000 pf	DC102K	Erie
C57	1.0 uf	CSR13E105KS	
C85 thru C88	2.2 uf	CSR13E225KS	
C60 thru C63	680 pf	C320C681K2G5CA	Kemet
C64, C65	2700 pf	B6A272J	Elpac

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C66 thru C70	: 2200 pf	B6A222J	"
C71, C72	: 0.015 uf	C330C153K1G5CA	Kemet
C73 thru C76	: 1.0 uf	C330C105K1G5CA	"
C77, C78	: 0.047 uf	C330C473K1G5CA	"
C79, C80	: 47 pf	C312C470K2G5CA	"
C89, C90	: 1800 pf	B6A182J	Elpac
C91, C92	: 0	none	

Timing and Multiplier Board (ref. dwg. SIE 39115723):

Component No.	: Value	Part No.	Source
C1	: 1.0 uf	C330C105K5R5CA	Kemet
C2	: 0.01 uf	C330C103K1G5CA	"
C3, C4	: 2.2 uf	CSR13E225KS	
C5	: 5.6 UF	CSR13E565KS	
C6	: 2200 pf	B320C222K2G5CA	Kemet
C7	: See sheet 3 of dwg. SIE 39115723		"

5.0 Digital Processor Subsystem

5.1 SUMMARY

NASA, JSC in Houston,Tx has developed a real-time signal processor for the fan beam scatterometer system. The software system has been designed and written to process in real time two quadrature channel pairs of radar scatterometer signals from the NASA L (1.6 ghz) or C (4.75ghz) band systems. The software has been implimented and tested in both L and C band flight systems using recorded radar and NERDAS (NASA Earth Resources Data Annotation System) signals as input data sources.

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6.0 SYSTEM ARCHITECTURE AND OVERVIEW

6.1 Microcomputer Hardware

The microcomputer hardware for the system resides on 2 wire-wrap boards. These boards have been designated the Accumulator and Controller boards. They reside in a card cage seperate from the ana- log subsystem in the PSD processor unit. Each of the microcomputer boards contains a microcomputer system based on the Intel 8085A-2 microprocessor, the Intel 8755A-2 EPROM and I/O combination and the 8156A-2 RAM (Random Access Memory) and I/O combination.

6.6.1 Accumulator Board

Figure 6.1 shows the block diagram for the Accumulator board. Basicly the board consists of 2 dual-port memories, each 4K x 8 in size, and the microcomputer system. Data inputs to this board come from the PSD processor analog subsystem. Inputs consist of 2,23 bit parallel channels and 2 discrete inputs, data valid and new frame. Data is output from the accumulator to the controller board via the dual port memories. The control of the dual port memories is maintained by the microcomputer on the Accumulator board. At all times one dual-port memory is mapped to the accumulator and one to the controller.

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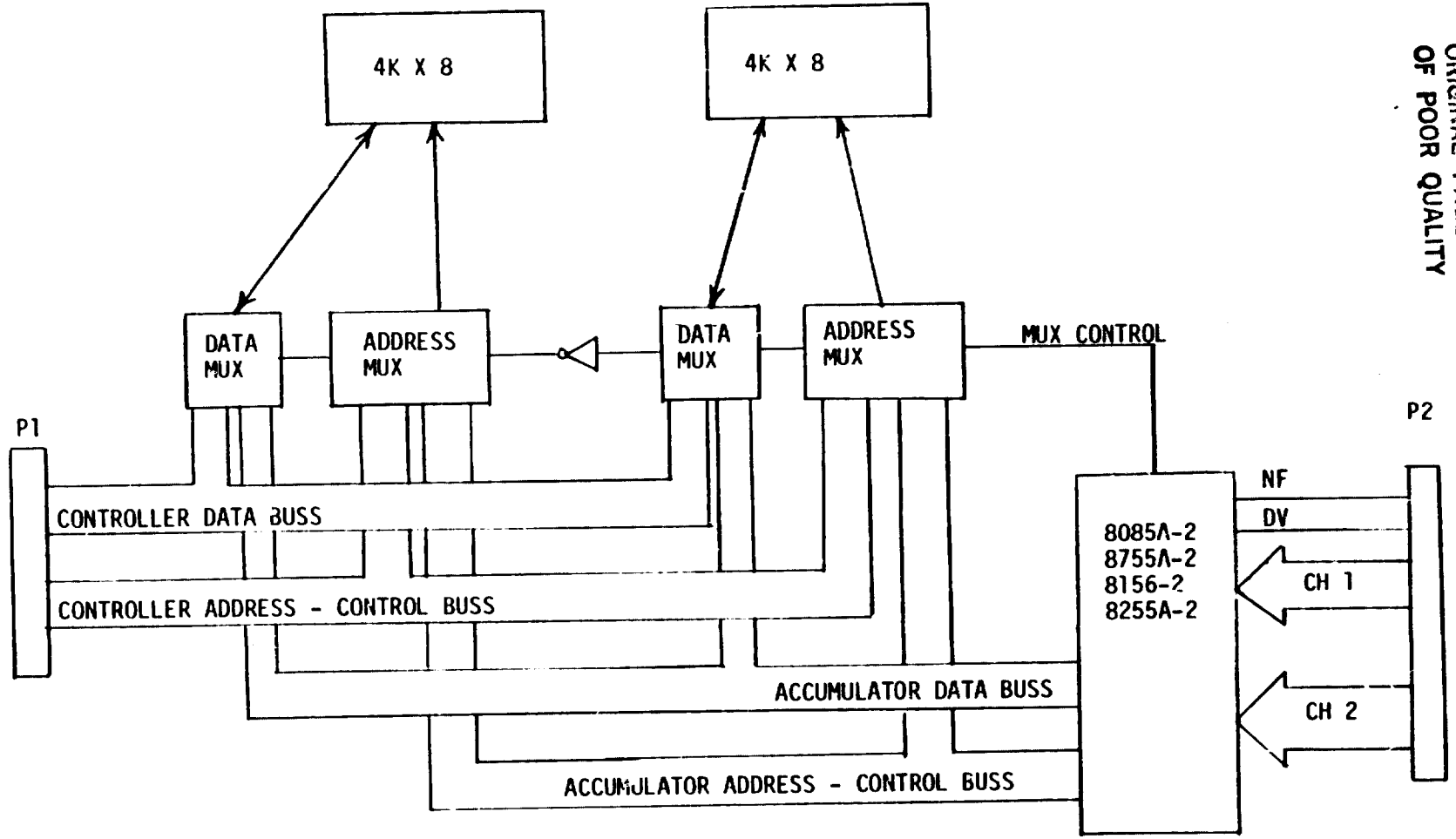

FIGURE 6.1 - ACCUMULATOR BOARD

6.1.2 Controller Board

A block diagram of the controller board is shown in figure 6.2. The controller board interfaces to the front panel,dual-port memories, NERDAS (NASA Earth Resources Data Annotation System), and tape recorder.

For diagnostic purposes an interface to a CRT terminal and LED displays are also provided. During run time operation data inputs come from the dual-port memories and the NERDAS interface. The input data is then output to a tape recorder in a 100khz pcm format. In diagnostic mode a serial channel operating at 1200 baud provides communication with a CRT terminal. This is similar to RS-232c format , the exception being the logic levels are TTL compatible. The front panel interface provides the capability to read the 2 push button switches,RUN and SELF TEST, and to turn on or off the 6 LED's (RUN,SELF TEST,NERDAS,NOISE,SIGNAL/NOISE and CPU ERROR).

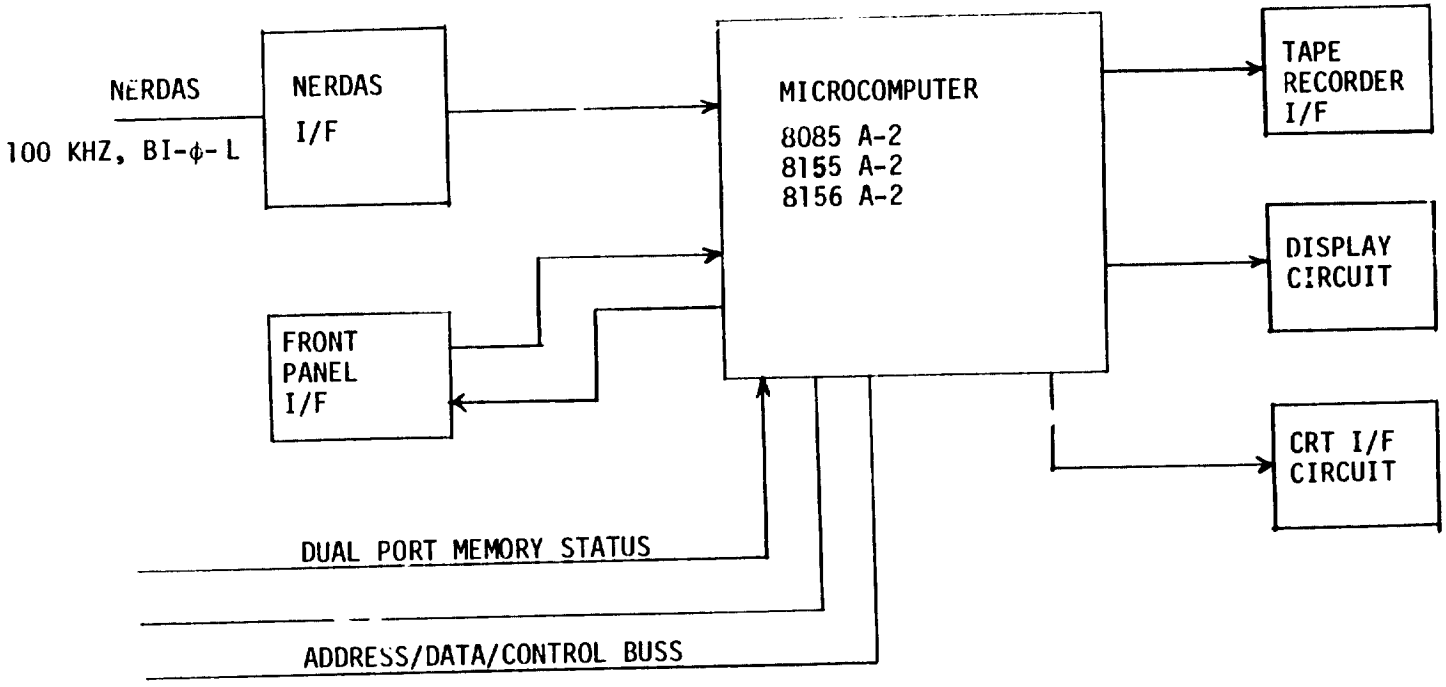

FIGURE 6.2 - CONTROLLER BOARD

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6.2 Microcomputer Software

All PSD Processor software has been developed using an Intel MDS-230 Development system. The language used is 8085 assembly language, using the Intel assembler, ASM80. All software is physically located in the 8755A-2's EPROM section.

6.2.1 Accumulator Software

The accumulator software is driven by 2 interrupts, Data Valid and New Frame. Figure 6.3 demonstrates the overall function of the accumulator board. The accumulator reads the channel 1 and 2 PSD values from the Analog processor subsystem and accumulates (adds) records for a 0.5 seconds. The accumulated PSD's are read by the controller board via the dual-port memories. There are 512 PSD's per record on each channel, each PSD being 23 bits wide. The accumulator reserves 32 bits for each accumulated PSD value in memory. For the C-band unit, 10 records are accumulated in 0.5 sec. and 5 records are accumulated in 0.5 sec. for the L-band.

6.2.2 Controller Software

- PROCESSOR RECEIVES NEW FRAME INTERRUPT
  - SET PSD POINTER TO START BUFFER
  - IF RECORD AVERAGE COUNT = (10 FOR C-BAND)
    (5 FOR L-BAND)
    - SWITCH DUAL PORT MEMORY
    - SET RECORD AVERAGE COUNT = 0
    - ENABLE INTERRUPT
    - HALT PROCESSOR
  - INCREMENT COUNT BY 1
  - ENABLE INTERRUPT
  - HALT PROCESSOR

- PROCESSOR RECEIVES DATA VALID INTERRUPT
  - ENABLE INTERRUPT
  - ADD 23 BIT CH 1 PSD TO VALUE POINTED TO BY PSD POINTER
  - INCREMENT PSD POINTER
  - ADD 23 BIT CH 2 PSD TO VALUE POINTED TO BY PSD POINTER
  - INCREMENT PSD POINTER
  - HALT PROCESSOR

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FIGURE 6.3 - ACCUMULATOR SOFTWARE

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As the name implies, the controller board controls the operation of the digital processor subsystem. This includes the front panel switches and LED's,NERDAS interface,tape recorder interface and interrupt enable on the accumulator board. The controller board has 2 basic modes of operation, selectable by the user, the RUN mode and the diagnostic mode (used for trouble-shooting). Figure 6.4 shows the operation of the run mode software. The run mode program was designed to allow operation of the PSD processor with a minimum of operator intervention. In essence, all that is required of an operator is to select either run mode or, in case of problems, diagnostic mode. Simply put, the run mode program gathers data from the NERDAS interface and accumulated PSD's from the dual port memories and transmits them in 100khz pcm format to a tape recorder. Signal to noise ratio of the PSD data is tested for a minimum of 10db in channel 0. If the 10db minimum is not met, the S/N LED is turned on until the required ratio is found.

The diagnostic mode software is a monitor program which communicates through a 1200 baud serial port to a crt terminal. This moniter program has many commands which are useful in trouble-shooting situations. A description of the moniter commands can be found in figure 6.5.

- TURN ON RUN LED
- WAIT FOR ACCUMULATOR TO SWITCH DUAL-PORT MEMORIES
- READ ONE SUBFRAME OF NERDAS DATA
- CALCULATE THE SIGNAL TO NOISE RATION OF DATA IN CH-2
- IF S/N < 10 db, TURN ON S/N LED ON FRONT PANEL
- OUTPUT NERDAS AND PSD VALUES TO TAPE
- READ SELF TEST SWITCH
- IF SELF TEST IS ON THEN:
  - TEST NOISE FLOOR DATA.
  - IF NOISE IS > 23.2 db, THEN FLASH NOISE LED
  - SEQUENCE THROUGH ALL LED's - TURN EACH ON FOR ≈ 1 SEC
- GOTO START

FIGURE 6.4 - CONTROLLER SOFTWARE - RUN MODE

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TABLE OF MONITOR COMMANDS

1. Display PSD.----- displays the PSD values in 32bit hexadecimal format. Command format D(channel no.-0 or 1) (starting address -three digit hex)(ending address- three digit hex :range-000-200)

2. Display Memory--- displays the 256 byte RAM in the 8156A-2. Command foramt M(carriage return).

3. Subroutine call-- calls a subroutine at user supplied address. Command format S(address-- 4 digit hex :range 0000-FFFF)

4. Goto run mode--- begins execution of the run mode program. Command format R(carriage return)

5. LED test ------- cycle through the front panel LED'S turning each on for approx. 1 second. Command foramt O(carriage return).

6. Clear PSD's ---- clears, sets to 00, all PSD memory under controller board control. Command format C(carriage return).

Figure 6.5 - TABLE OF MONITOR COMMANDS

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7.0 Detailed Design and Theory of Operation

7.1 Accumulator Board Hardware

The schematic diagram for the accumulator circuitry is shown on drawing SEE39115193 sheets 3,4 and 5. The circuit is constructed on a Mupac wire-wrap board, model 3244890-03. When power is applied, program execution will begin from address 0000. This is insured by the R-C network, R1-C1, which holds cpu RESET low until the 5V supply is stable. The EPROM in the 8755A-2 is located at address 0000H. As shown on the schematic, the 8755A-2 is selected when address line A15 is 'low' and address line A11 is 'low'. Since the memory is not fully decoded it will appear at all address's where A15 and A11 are logic '0'. Address decoding for the 8155A-2 is done in a similar manner as the 8755. The chip select is 'true' when A12 is 'true'. This allows the 8156 RAM to be addressed at 2800H and presents no conflict with the 8755 EPROM. The 8156 RAM is 256 bytes (100H) and ranges from 2800H to 28FFH. The 8755 EPROM is 2K bytes (800H) and ranges from 0000H to 07FFH. The dual port memory is addressed at 8000H to 8FFFH, which is 4K bytes. The dual port memory will be selected at any address in which A15 is 'true'. This spans the range of 8000H to FFFFH. By only addressing it at 8000-8FFFH conflict with the 8156 RAM is avoided. I/O decoding is similar to memory decoding described above. The I/O ports used on the 8755 are: 0-input for PK-16 thru PK-22, 1-input to read dip switch, 2- data direction register for port 0, 3- data direction register for port 1. These

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ports are selected when A15 and A11 are 'low' and IO/M is 'low', then AD0 and AD1 select 0,1,2 or 3. The I/O ports for the 8156 are addressed at 28-2BH. Port 28 is the command/status register, 29H is the input for PK0-PK7, 2AH is the port for PK8-PK15, port 2BH is used to output the MUXEN signal to switch dual port memories. The I/O ports on the 8255A-2 are addressed to locations 48-4BH. Ports 48-4AH are inputs and are use to read PJ0-PJ26. Port 4BH is the control register for the 8255.

There are 2 dual-port memories on each accumulator board. These memories are 4096 bytes long, addressed to 8000H-8FFFH as noted above. Each of the dual-port memories can be addressed by either the accumulator or the controller. The 8085 on the accumulator board controlls the state (i.e. which of the memories is controlled by the accumulator and which is controlled by the controller) of the memories via a output line on the 8156, MUXEN. The address and control line multiplexing is done with 74LS157N's, with one set (U13,18,23,28) being controlled by MUXEN/ and the other (U12,17,22,27) controlled by MUXEN. Data multiplexing is accomplished through the use of Intel 8216 bi-directional bus-drivers. Data direction control is done by using the multiplexed memory read (MRD/ and XRD/) to set the direction control line on the 8216, pin 15. The destination, controller or accumulator, control of the data bus is determined by MUXEN and MUXEN/.

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7.2 Controller Board Hardware

The schematic diagram for the controller board electronics is found in drawings SEE39115194, sheets 3-6. The circuit is constructed on a Mupac wire wrap board, model 3244890-03. The heart of the controller board is the 8085 microcomputer discussed in section 6.1.6. The memory and I/O port addresses for the 8755 and 8156 chips are identical to those used on the accumulator board. The 8755 is used to interface the NERDAS decom circuit. The 8156 is used to interface the front panel and tape recorder output circuit. An interface to a CRT terminal is provided by using the Serial Input Data line (SID) and the Serial Output Data line (SOD) on the CPU chip. R16,D1 and D2 provide vide a means of converting RS-232 signals to TTL compatible levels. The CPU reset is connected to a front panel switch which can ground this line and reset the CPU. U5 is an 8 bit latch used to de-multiplex the address lines A0-A7. Sheet 4 of the controller schematic shows the tape recorder output circuit, discrete inputs and front panel interface. The tape recorder interface provides a means of converting 8 bit parallel data to 100khz Bi-phase-L serial data. Figure 7.1 is a timing diagram of the interface timing for data input. The data is written to the S2350 USART via the 8156 I/O lines, TD1-TD8. The S2350 accepts two types of input words ,fill words and data words. The fill words are used to provide a continous

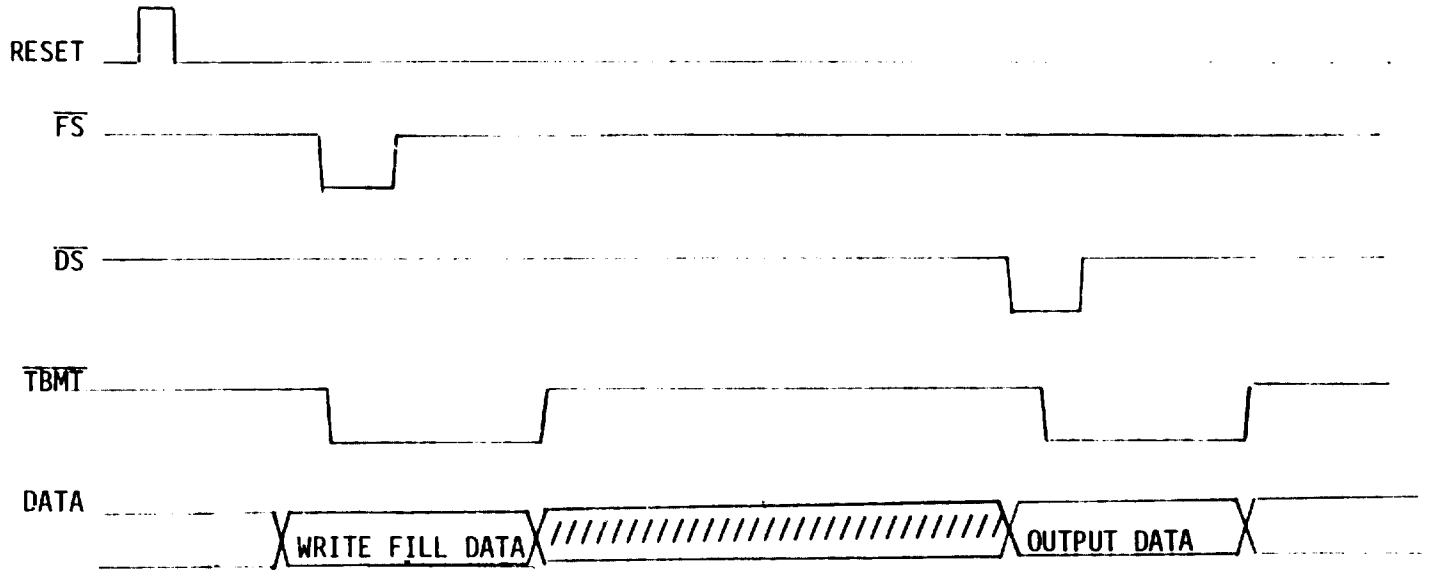

FIGURE 7.1 - TAPE RECORDER INTERFACE TIMING

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output in the cases when no data is being transmitted. The fill words are loaded into a fill register in the USART when FS/ is logic '0'. Data words are loaded into the data register of the USART when DS/ is logic '0'. The transmission of data will always take place when 'fresh' data is in the data register. At 100k bits/second and 8 bits/character it works out that new data must be written to the USART every 80 us or a fill word will be transmitted.

The front panel interface is controlled through I/O lines on the 8156 chip. There are three output lines, FPA1,FPA2 and FPA3, and two input lines, RUN and SELF TEST. The output lines go to U11, a 3 to 8 decoder which determines which of 6 LED's is illuminated. Note that at all times either the RUN or RUN/ LED will be on and when the NERDAS LED is on it will flash due to U30, a 555 timer. The two input signals originate at the front panel on the RUN and SELF TEST switches. When the switch is depressed the coesponding signal, RUN or SELF TEST, will be taken to ground or logic '0'. There are 2 pull-up resistors on the controller board, R6 & R7, which keep these lines at Vcc or logic '1' when the switch is not pressed.

Sheet 5 of the controller board schematic shows the NERDAS interface. This interface inputs a 100khz Bi-phase-L serial data stream and converts this to 8 bit parallel words which are read by the CPU through the 8755 I/O lines. Figure

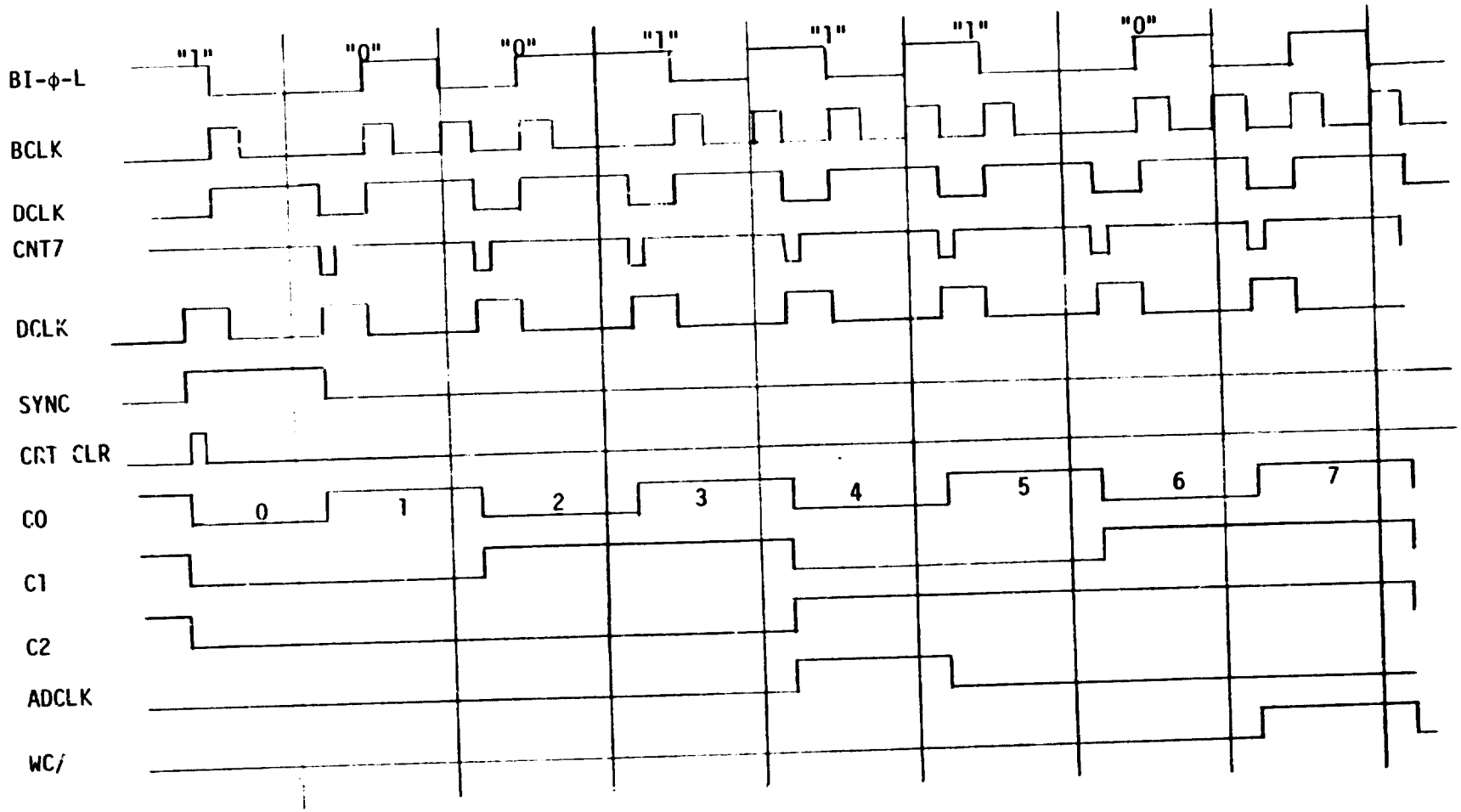

FIGURE 7.2 - NERDAS INTERFACE TIMING

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7.2 is a timing diagram for this interface. The NERDAS data is input by U19, a opto-isolator, which maintains isolation between NERDAS ground and the PSD processor ground. Since U19 inverts the data, an inverter, U20, is used to restore the original polarity. At this point the Bi-phase-L data goes to a latch, U28, and to 2 retriggerable multivibrators, both haves of U24. One half of U24 produces a 2us pulse on the positive going edges and the other produces a 2us pulse on the negative going edge. These two pulse streams are or'ed together by U25 to produce a series of 2us pulses for every transition of the Bi-phase-L data, see BCLK, on timing diagram. On the rising edge of BCLK the Bi-phase -L data is latched into one half of U28 and a '1' is latched into the other half whose output is DCLK and DCLK/. When DCLK goes high U15 is enabled to count. The 1mhz clock generated by U12 clocks U15 every 1us. When the count of U15 equals 7, the CNT7/ goes low and clears the DCLK to a low. This in turn clears U15 to an all zeros count and CNT7/ goes to a high level. It is important to note at this time that for U15 to reach a count of 7, at least 6 microseconds must pass worst case. This insures that the circuit will lock on the correct BCLK edge since BCLK pulse's can occur at 5 us intervals. The latched Bi-phase-L data is input by the shift register U26, a 74LS164, on the rising edge of DCLK/. The serial output of U26 is input by another shift register, U27-74LS96, also on the rising edge of DCLK/. The parallel outputs of these shift registers is tested for the sync word, FDF, by U21,22,23. When the sync is detected the SYNC DETECT

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signal is output which clears the NERDAS word count to 00 and sets the bit counter ,U29, to 00. DCLK continues to increment the bit counter and at a count of 4 bit times after sync is found, the NERDAS address is incrememted and NERDAS data is latched into the output registers ,U33 & U34. When the bit count equals 7,(eight bit times from 0-7), WC/ goes low and will cause the counter U29 to clear on the next DCLK rising edge. This in turn causes WC/ to go high until another 8 bit times goes by.

C-2

7.3 Accumulator Board Software

The accumulator software was developed on a Intel MDS-230 develpoment system using the Intel macro assembler, ASM80. Assembly language was chosen for this project due to the real-time processing speed required. The accumulator program source is named CBAND.SRC for both C-band and L-band processors. The L and C band programs are identical except for a one byte record average count which will be discussed later.

Upon power on, the CPU begins execution from address 0000. At this location is a jump to an initialization routine, see listing 7.1. This routine configures the 8156,8755 and 8255 as per table 7.1.

DEVICE	PORT	ASSIGNMENT	ADDRESS
8755	A	INPUT	00H
	B	INPUT	01H
8156	A	INPUT	29H
	B	INPUT	2AH
	C	OUTPUT	2BH
8255	A	INPUT	48H
	B	INPUT	49H
	C	INPUT	4AH

ACCUMULATOR I/O PORT DEFINITION

TABLE 7.1

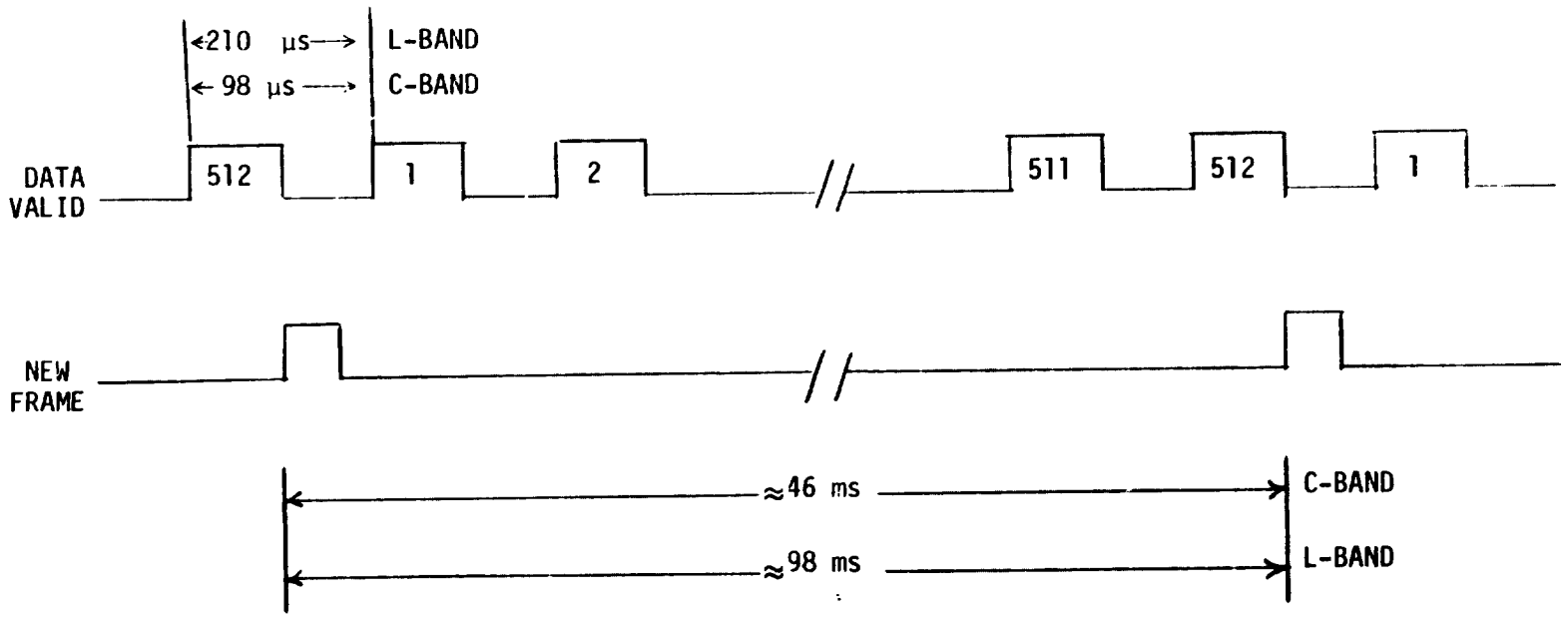

FIGURE 7.3 - DATA VALID AND NEW FRAME TIMING

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The actual accumulation program is entirely interrupt driven. There are 2 interrupts that drive the program, DATA VALID and NEW FRAME. Figure 7.3 shows the timing relationship between these signals. They are generated on the Analog Processor Subsystem timing and control board. For every frame of data there are 512 data valid interrupts and one new frame interrupt. A frame is defined as the output of the 512 point chirp-Z-transform, equivilent to a 512 point FFT. Each of the 512 points is a 23 bit power spectral density (PSD) value. Both C and L-band processors are dual channel units and must accumulate 2 PSD values for every data valid interrupt.

The accumulation process begins with the new frame interrupt, RST 5.5. At this time the buffer pointer is reset to start of buffer, stack pointer is set to a none existent memory location and the record count is tested for a count of 5 if L-band or 10 if C-band. If the count value is reached then the dual port memories are switched, allowing the controller board to access the newly accumulated PSD's and providing the accumulator with an initialized (all zeros) accumulation buffer. If the count value was not reached then the count is incremented. In both cases, upon completion of the New Frame interrupt routine, interrupts are enabled for data valid interrupt and the CPU is halted. The Data Valid interrupt, RST 7.5, initiates the accumulation loop which adds PSD(n) of the current frame to PSD(n) of the past frame. This results in the addition of

multiple frames of PSD data for averaging purposes. The PSD's are to be accumulated for 0.5 sec. which is 5 frames for L-band data and 10 frames for C-band data. Figure 7.4 is the accumulation buffer defination map.

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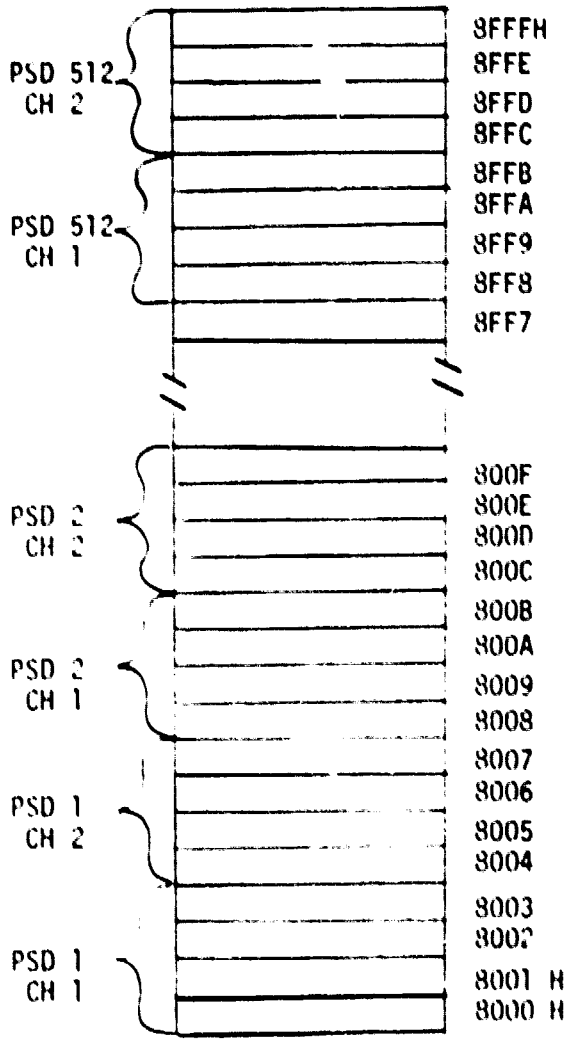

FIGURE 7.4 - ACCUMULATION BUFFER DEFINITION

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7.4 Controller Board Software

The controller board software consists of two main programs, a diagnostic monitor called MONITR.ASM and a run time program called RUN.ASM. These programs were both developed on the Intel MDS-230 system and were written in 8085 assembly language using the Intel ASM80 macro assembler. Please refer to listings 7.2 and 7.3 for the following discussion of the controller software. MONITR.ASM is originated at location 0000H and ends at location 04ABH. RUN.ASM begins at 0500H and ends at 07CEH. On power on, program execution begins at location 0000H, which is the start of MONITR. At this location is a jump to the initialization routine,INIT. INIT programs the I/O devices to the state shown in table 7.2.

DEVICE	PORT	ASSIGNMENT	ADDRESS
8755	A	INPUT	00
	B	INPUT	01
8255	A	INPUT	0CH
	B	INPUT	0DH
	C	INPUT	0EH
8156	A	OUTPUT	29H
	B	INPUT	2AH
	C	OUTPUT	2BH

CONTROLLER I/O PORT DEFINITION
TABLE 7.2

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Upon completion of the initialization, the program waits for either the run switch or self test switch to be pushed by the operator. If the run switch is pressed then the RUN program is run. If the self test switch is pressed then the program MONITR is run.

7.4.1 Controller Monitor Program

The controller monitor,MONITR, is run when the self test switch is pressed immediately after a reset or power on, as noted above. This moniter was designed to be a development aid during the design phase of the project. It can also be a help if problems (heaven forbid !) should ever arise. A list of the moniter commands can be found in figure 6.5. The monitor communicates with a crt terminal through an DB-25 connector on the back panel of the chassis. The terminals that are known to work with this system are the Lear-Siegler ADM-3 and Beehive model DM10. There could be a problem with some other terminals due to the TTL level transmit line as opposed to true RS-232C levels. The only signals required for operation of the serial interface are XMIT,RCV and logic ground. The baud rate is 1200, with 1 start bit, 1 stop bit and no parity.

7.4.2 Using the Monitor

As noted above , a table of monitor commands is given in figure 6.5. The individual commands are given below in

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some detail. In each case the operator must wait for the prompt character, *, before entering the command. In the explaination of each command the command letter is shown in some cases with numbers, which may be seperated by a comma. These numbers are always assumed to be in hexadecimal radix, as either a 3 or 4 digits, as specified by the command.

1. The D (display PSD's) command. The D command allows the operator to view the contents of the PSD buffer in hexadecimal format. The command form is:

D(channel)(starting PSD),(ending PSD)

For example, display from channel 0, PSD's 000-010. The operator would enter:

D0000,010(cr)

The monitor will output:

```
000 000 00000000 00000000 00000000 00000000
004 004 00000000 00000000 00000000 00000000
008 008 00000000 00000000 00000000 00000000
012 00C 00000000 00000000 00000000 00000000
*
```

Notice that the first PSD address is in decimal, the second address is hexadecimal. These are followed by 4 32 bit PSD's ,4 bytes each, in hexadecimal format. Upon completing the D command, the * prompt is output.

2. The M (display 256 byte scratch ram) command. The M command takes the form:

M(cr)

The memory is displayed from address 2800 hex., and continues for 16 display lines. Each display line takes the form shown below

aaaa h h h h h h h h h h h h h h h h ccccccccccccccc

Where aaaa is the display address in hexadecimal, and h represents data present in memory starting at aaaa. The ASCII characters starting at aaaa are given at the right (represented by the sequence of c's), where non-graphic characters are printed as a (.) symbol.

3. The S (call subroutine) command. Program execution is transfered to a subroutine via a call instruction. The S command takes the form

Saaaa(cr)

Where aaaa is the 16 bit hexadecimal address of the subroutine to be called. Console control will be restored upon completion of the subroutine called.

4. The R (execute run mode) command. Program execution is transfered to address 0500H, which begins the run mode operation. Console control will not be returned to the user. The R command takes the form

R(cr)

See 7.4.4 for details on run mode operation.

5. The O (front panel LED test) command. This command takes the form

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O(cr)

All front panel LED's are turned on in sequence.

6. The C (clear all memory) command. This command takes the form

C(cr)

All RAM memory in the system will be cleared(set to 0) including the scratch RAM. Console control is restored by pressing the SELF TEST switch after this command.

7.5 Controller Run-Time Software

The controller run-time software is divided into two sections, the RUN program and SELF TEST program. The operator can determine which of these programs the system will run. On power on or immediatly following a reset, either the RUN or SELF TEST switch may be depressed, depending upon which function is desired. The RUN program is the normal operating mode for the system while collecting flight data. SELF TEST is used as a confidence check for the entire system.

When in the run mode, the following sequence of operations will occur for every accumulated data record.

1. WAIT FOR DUAL-PORT MEMORY CONTROL LINE TO CHANGE STATE, THIS SIGNIFIES THE ACCUMULATOR HAS COMPLETED AN ACCUMULATION CYCLE, AND GOOD DATA IS NOW IN THE DUAL-PORT MEMORY ADDRESSED BY THE CONTROLLER.

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2. READ ONE SUBFRAME OF NERDAS DATA INTO NERDAS BUFFER. SEE FIGURE 7.5 FOR A DESCRIPTION OF THE NERDAS BUFFER.
3. TEST FOR THE SIGNAL/NOISE RATIO TO BE GREATER THAN 10 DB.
4. OUTPUT THE NERDAS DATA BUFFER AND THE PSD BUFFER TO THE TAPERECORDER. SEE FIGURE 7.6 FOR A DESCRIPTION OF THE PSD BUFFER AND OUTPUT DATA FORMAT.
5. READ THE SELF TEST SWITCH. IF THE SWITCH IS DEPRESSED THEN RUN SELF TEST , OTHERWISE GOTO STEP 1.

The operator should be aware that when an error condition is found by the processor, the appropriate front panel LED will light. The absence of NERDAS data will cause the NERDAS LED to flash at approximately a 1 Hz rate, while a bad (<10db) signal-to-noise raito will cause the S/N LED to light continiously while the error condition occurs. When the CPU ERR. LED is lit, the operator must reset the system and press RUN to continue collecting flight data.

When in the self test mode, the following sequence of operations will occur before the program returns to the run mode of operation.

1. Wait for the dual-port memory control line to change state twice. Allows self test data to be accumulated in dual port memory.
2. Test the system noise floor to be less than 22db.
3. Test for the signal/noise ratio to be greater than 10db.
4. Perform LED test. Cycle all LED's on-off.

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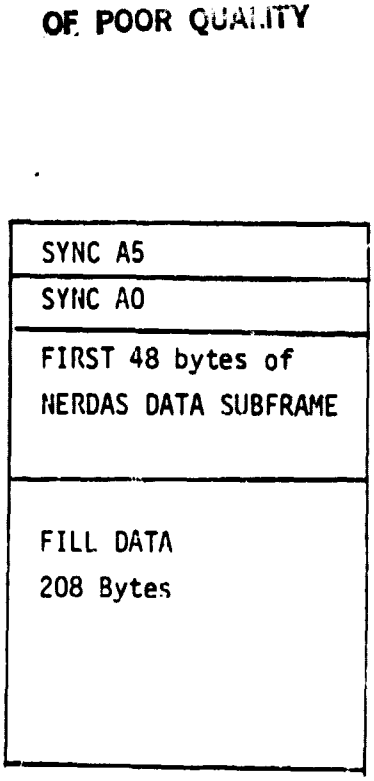

Figure 7.5 - NERDAS BUFFER SUBFRAME

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WORD 0	SYNC WORD A5
	SYNC & SUBFRAME AX*
	CH 1 PSD(N**) BYTE 0 (LSB)
	CH 1 PSD(N) BYTE 1
	CH 1 PSD (N) BYTE 2
	CH 1 PSD(N) BYTE 3 (MSB)
	CH 2 PSD(N) BYTE 0 (LSB)
	CH 2 PSD(N) BYTE 1
	CH 2 PSD(N) BYTE 2
	CH 2 PSD(N) BYTE 3 (MSB)
	CH 1 PSD(N + 1) BYTE 0(LSB)
	CH 1 PSD(N + 31) BYTE 0
	CH 1 PSD(N + 31) BYTE 1
	CH 1 PSD(N + 31) BYTE 2
	CH 1 PSD(N + 31) BYTE 3
	CH 2 PSD(N + 31) BYTE 0
	CH 2 PSD(N + 31) BYTE 1
	CH 2 PSD(N + 31) BYTE 2
WORD 257	CH 2 PSD(N + 31) BYTE 3

*X = SUBFRAME 0 - F

**N = 32*X

FIGURE 7.6-A - PSD DATA SUBFRAME FORMAT

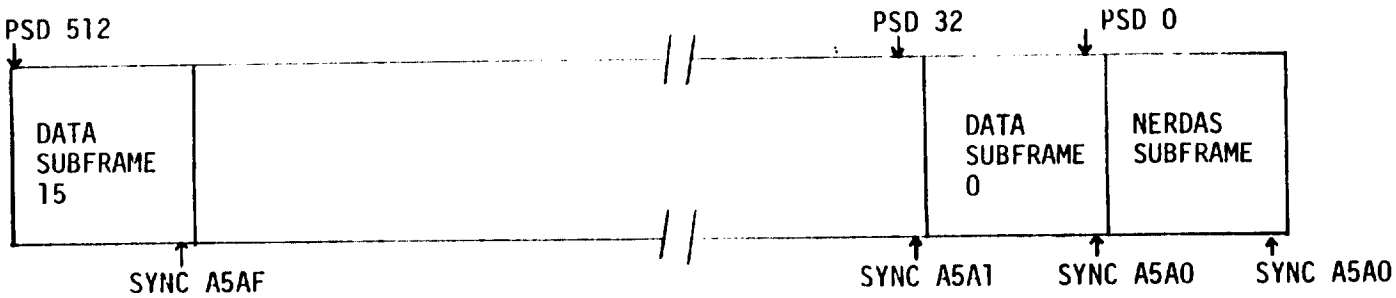

Figure 7.6-B - OUTPUT DATA FORMAT

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5. Return to run program.

When in self test, the operator must hold the self test switch down **continuously** until self test has ended. While the self test switch is depressed, a test signal is injected into the analog processor. This signal is of known amplitude and frequency so that system performance can be measured against it. If either the signal/ noise or noise floor test fails, the corresponding front panel LED will flash until the system is reset.

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8.0 Operations Guide

The PSD processor has been designed for a minimum of operator attention. There are no adjustments or calibrations to be made onboard the aircraft during operation.

Upon powering the system up, you will notice that the error indicator LED labeled "CPU ERR" will be lit. This is a normal condition on power up, indicating that the processor is awaiting a command to enter either run mode or self test. At this point the operator should press the self test switch, holding the switch down during the test, and the processor will self test. Proper operation of the system is indicated by all LED's being sequenced on-off one time. If an error condition is detected, the error indicator will flash continously. If this occurs the unit may need servicing before flying.

After passing the self test or upon depressing the RUN switch, the processor will be in RUN mode operation. This is done by pressing the RUN switch. When in RUN mode, the RUN LED above the RUN switch should be lit. If, at this time there is no scatterometer signal or a bad signal, the S/N (signal-to-noise ratio) LED will be lit. This indicates a signal- to-noise ratio of less than 10db. If this indication occures during a data take

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then there is a problem with the RADAR system or cables and corrective action needs to be taken. When the NERDAS LED is lit the processor is not getting a good NERDAS signal. The NERDAS LED will flash during the time NERDAS is out. At this time the data output will change from a 2 Hz frame rate to 1 Hz frame rate. If at any time during run mode the CPU ERR led should be lit, the operator should reset the system and proceed as though just powered up. Should the CPU ERR LED stay lit, the unit is nonfunctional and should be serviced.